(19)日本国特許庁（ＪＰ）　(12)公開特許公報（A）　(11)特許出願公開番号

特開平11－306132

(43)公開日　平成11年(1999)11月5日

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// Ｈ０４Ｎ　7/16		Ｈ０４Ｎ　7/16	Ａ

審査請求　未請求　請求項の数6　ＯＬ　（全 13 頁）

(21)出願番号　特願平10－108065

(22)出願日　平成10年(1998)４月17日

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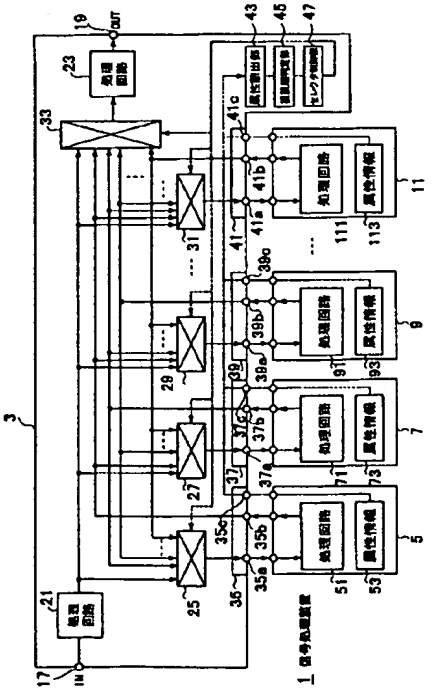
(54)【発明の名称】　信号処理方法及び信号処理装置並びにディジタル放送受信装置

(57)【要約】

【課題】　第１の装置の任意のポートに第２の装置を接続しても、自動的に優先順位を判定して、優先順位に従ったデイジーチェーン接続を行う。

【解決手段】　複数のポート３５、３７、３９、４１を有する第１の装置３と、各ポートに任意に接続可能な第２の装置５、７、９、１１からなる信号処理装置１において、各ポートに対応して、少なくとも他の全てのポートからの入力信号を択一して該ポートに対する出力信号とする第１のセレクタ２５、２７、２９、３１と、少なくとも全てのポートの入力信号から択一して出力信号とする第２のセレクタ３３とを設け、各ポートに接続された第２の装置の属性情報を属性読出部４３で読出し、接続順判定部４５で属性情報に基づいて接続優先順位を判定し、この判定に基づいてセレクタ制御部４７よりセレクタ２５、２７、２９、３１、３３を制御し、優先順位に従ったデイジーチェーン接続する。



理されたデータを共通処理ユニットCに供給することになる。

この実施例では入力データを処理する機能を有する処理ユニットとして処理ユニットP_1と、単なる伝送を行う線路として構成した処理ユニットP_2と、共通処理ユニットCとを用いているが、より多い処理ユニットを用いることができることは第1図について説明したとおりであり、この際には上記のように2値のモード制御信号および1つのインバータのみを備えるデコーダDに代えて第1図に示したように複数桁からなるモード制御信号とこれを復号するデコーダを用いればよい。

〔発明の効果〕

本発明によれば、処理すべきデータについての入力ピンの数として入力端子数が最大の処理ユニットの入力端子の数で足り、これにこの処理ユニットをデコーダを介して選択するに必要なモード選択信号の入力ピンを加えればよいから、入力ピンの数に制約されることなく、多くの処理ユニットを1つのＬＳＩ上に用意しておくことができ、多品種を1種類のＬＳＩで実現できるという格別の効果が達成される。

4.図面の簡単な説明

第1図は本発明の原理を示す図、

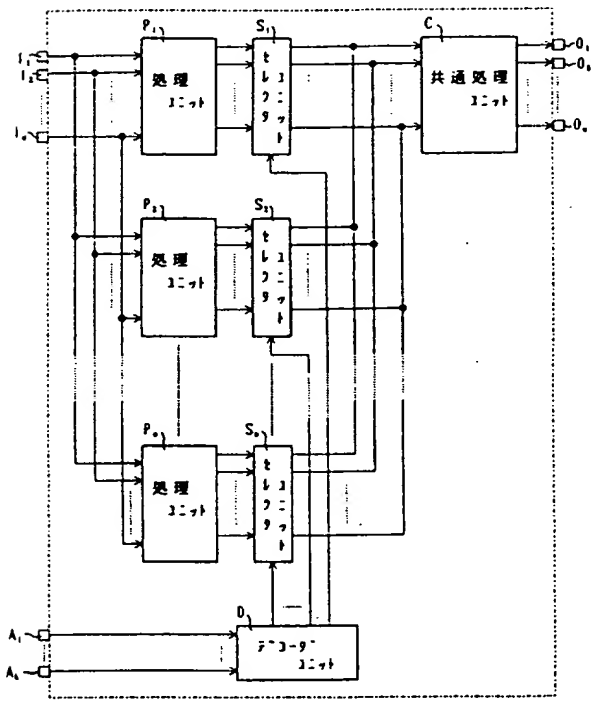
第2図は本発明の実施例を示す図である。

特許出願人　富士通株式会社

代理人　瀧野秀雄

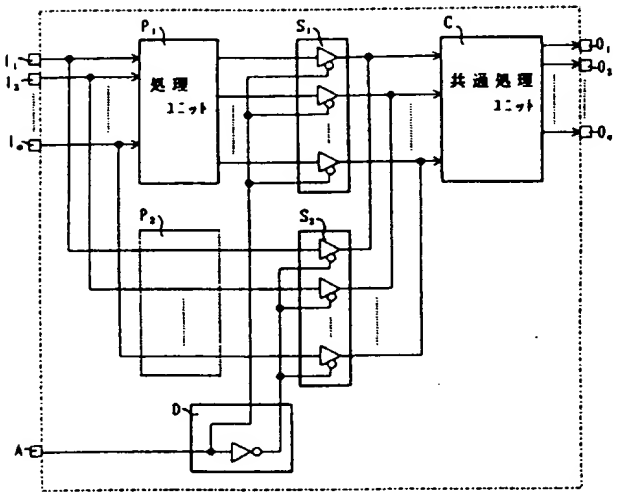
同　中内康雄

同　有坂悍



原理図

第1図



実施例

第2図

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号
特開2002－164849
（P2002－164849A）
(43)公開日　平成14年６月７日(2002.6.7)

(51)Int.Cl.⁷	識別記号	ＦＩ		テーマコード（参考）
Ｈ０４Ｂ　10/02		Ｈ０４Ｑ　3/52	Ｃ	５Ｋ００２
Ｈ０４Ｊ　14/00		Ｈ０４Ｂ　9/00	Ｔ	５Ｋ０６９
14/02			Ｅ	
Ｈ０４Ｑ　3/52				

審査請求　未請求　請求項の数２　ＯＬ　（全 ５ 頁）

(21)出願番号　特願2000－362674(P2000－362674)

(22)出願日　平成12年11月24日(2000.11.24)

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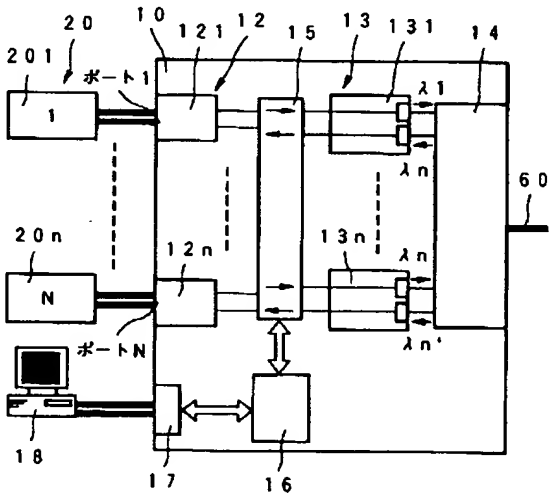
弁理士　川澄　茂

Ｆターム(参考)　5K002 BA06 DA02 DA09 DA13 EA03
FA01
5K069 BA09 CB10 DB07 DB33 EA24

(54)【発明の名称】　波長多重伝送装置

(57)【要約】
【課題】動的なネットワーク構成の変化に対応して、通信回線の内部の接続経路を変更することのできる波長多重伝送装置を提供すること。
【解決手段】通信回線に接続される複数の入出力ポート１～ＮとＷＤＭ光送受信モジュール１３１～１３ｎをマトリックススイッチ１５を介して接続すると共に、該マトリックススイッチ１５を制御するスイッチ制御回路１６とその通信ポート１７とを設け、外部から入力される通信回線の接続情報により、上記マトリックススイッチ１５の入出力ポート１～Ｎに対するＷＤＭ光送受信モジュール１３１～１３ｎの接続経路を変更し得るように構成する。



(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平11－177599

(43)公開日　平成11年(1999)７月２日

(51)Int.Cl.[6]	識別記号	ＦＩ	
Ｈ０４Ｌ　12/44		Ｈ０４Ｌ　11/00	３４０
12/28			３１０Ｚ

審査請求　未請求　請求項の数２　ＯＬ　（全５頁）

(21)出願番号　特願平9－346425

(22)出願日　平成９年(1997)12月16日

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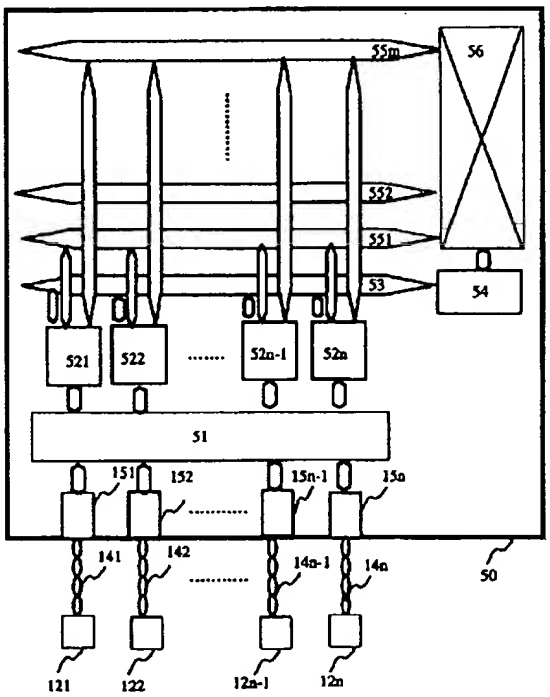
(74)代理人　弁理士　絹谷　信雄

(54)【発明の名称】　イーサネットリピータ

(57)【要約】

【課題】　スイッチングハブより安価で、複数のイーサネットＬＡＮ端末が同時にデータを送信できるイーサネットリピータを提供する。

【解決手段】　複数のポート１５１～１５ｎと、そのポート個数ｎより少ない複数のスイッチングを行うスイッチング部５６と、このスイッチング部５６によりスイッチングされる複数個の内部バス５５１～５５ｍと、これらの内部バス５５１～５５ｍにそれぞれ任意のポートを切り替え接続する切替接続部５２１～５２ｎとを備えた。内部バスを介してスイッチング部５６に接続された複数のポートは同時にデータ通信できる。



United States Patent [19]

Aoyama

[11] **Patent Number: 4,825,098**

[45] **Date of Patent: Apr. 25, 1989**

[54] **BIDIRECTIONAL SEMICONDUCTOR DEVICE HAVING ONLY ONE ONE-DIRECTIONAL DEVICE**

[75] Inventor: **Keizo Aoyama**, Yamato, Japan

[73] Assignee: **Fujitsu Limited**, Kawasaki, Japan

[21] Appl. No.: **130,630**

[22] Filed: **Dec. 8, 1987**

[30] **Foreign Application Priority Data**

Dec. 17, 1986 [JP] Japan 61-298887
Dec. 17, 1986 [JP] Japan 61-298895
Dec. 18, 1986 [JP] Japan 61-300112

[51] **Int. Cl.**[4] **H03K 3/01**; H03K 3/356; H03K 17/693; H03K 19/092

[52] **U.S. Cl.** **307/243**; 307/465; 307/475; 340/825.02; 340/825.43; 365/231; 365/154; 377/64; 364/716

[58] **Field of Search** 307/443, 465, 466, 467, 307/468, 469, 475, 542, 243, 246, 248, 571, 574, 575, 576, 585, 270, 279, 272.1, 296.1, 304; 365/205, 230, 231, 154, 78; 364/716; 377/64, 69, 74; 370/60; 340/825.02, 825.43

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4,621,201	11/1986	Amdahl et al.	307/243 X
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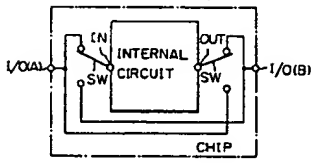
4,709,173	11/1987	Nishimichi et al.	307/243
4,774,422	9/1988	Donaldson et al.	307/243 X

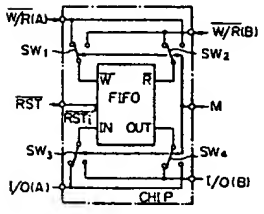
Primary Examiner—Stanley D. Miller
Assistant Examiner—David R. Bertelson
Attorney, Agent, or Firm—Staas & Halsey

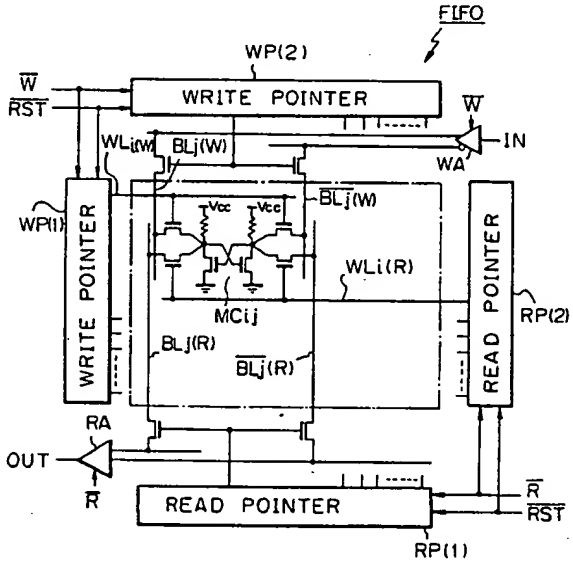
[57] **ABSTRACT**

In a one-directional internal circuit such as a first-in first-out (FIFO), switchover switches are provided between the internal input/output ports and external ports thereof, and the switches are controlled by a mode signal, thereby enabling a bidirectional data transmission within one chip.

8 Claims, 11 Drawing Sheets







	L #	Hits	Search Text	DBs
1	L1	183073	((i adj1 o) input$4 output$4) near20 (port pin pad)	USPAT; US-PGPUB
2	L2	13897	1 near50 ((select$5 reconfigur$4 configur$4) near20 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
3	L3	769	2 near50 ((process$3 core internal$2 inside (on adj1 chip)) near20 (resource element unit module device peripher$2))	USPAT; US-PGPUB
4	L4	11402	1 near20 ((select$5 reconfigur$4 configur$4) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
5	L5	452	4 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	USPAT; US-PGPUB
6	L7	21135	1 near20 ((select$5 reconfigur$4 configur$4 switch$3) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
7	L9	908	7 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	USPAT; US-PGPUB
8	L10	631	(pin port pad (i adj1 o) input$4 out$4).ab,ti. and 9	USPAT; US-PGPUB
9	L12	71320	((i adj1 o) input$4 output$4) near20 (port pin pad)	EPO; JPO; DERWENT; IBM_TDB
10	L16	4471	12 near20 ((select$5 reconfigur$4 configur$4 switch$3) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	EPO; JPO; DERWENT; IBM_TDB
11	L11	397	(pin port pad).ab,ti. and 9	USPAT; US-PGPUB
12	L17	158	16 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	EPO; JPO; DERWENT; IBM_TDB
13	L19	4902	12 near20 ((select$5 reconfigur$4 configur$4 switch$4 multiplex$3) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	EPO; JPO; DERWENT; IBM_TDB
14	L20	16	19 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2)) not 17	EPO; JPO; DERWENT; IBM_TDB
15	L21	23497	1 near20 ((select$5 reconfigur$4 configur$4 switch$4 multiplex$3) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
16	L22	1033	21 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	USPAT; US-PGPUB
17	L23	30	(pin port pad).ab,ti. and 22 not 11	USPAT; US-PGPUB
18	L24	292	22 and analog	USPAT; US-PGPUB
19	L25	202	24 not (11 23)	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	JP 2001251328 A	☐	MULTIPLEX PORT ETHERNET (R) UNIT, AND METHOD AND SYSTEM FOR MINIMIZING EXTERNAL PIN	
2	JP 2000035899 A	☒	EMULATION MODULE	
3	JP 04139933 A	☒	MULTIPLE ACCESS MULTIPLEX EXCHANGE SYSTEM	
4	JP 58047225 A	☒	METHOD AND DEVICE FOR CORRECTING TEMPERATURE FOR SOLID STATE SENSOR	
5	EP 518488 A1	☒	Bus interface and processing system.	
6	US 20020186046 A	☒	Semiconductor integrated circuit device for computer system, has interconnect structure with multiplexers which process multi-bit inputs from input ports to output port within semiconductor substrate	
7	KR 2002040430 A	☒	Apparatus and method for inspecting stocking of coil product in cold coil packing line	
8	US 6366997 B	☒	Processing method for manifold array processing element switch control, has PE to receive communication instruction to transmit control signal to multiplexer and to communicate information using data input and output	
9	US 20020026606 A	☒	Integrated circuit with embedded memory and on-chip testing circuit, has controller coupled to multiplexer to select subset of data lines among data lines of internal bus coupled to embedded memory device	
10	US 5617082 A	☒	Electronic access control device for industrial, commercial and residential use - has comparator that is electrically connected to processor for comparing at least one access code to value input received via input device	
11	RU 2035770 C	☒	magnetograph - has processor to organise interrogation of sensors and uses multiplexers to pass information to magnetic tape in order of interrogation	
12	EP 494831 A	☒	Optical processing device for optical telecommunication system - produces output signal with wavelength specified by wavelength of reference optical beam	
13	GB 2223867 A	☒	Multiprocessor data processing system - comprises network of communication device having I=O multiplexers with byte-wide ports for connection to ports of neighbouring units	
14	EP 125411 A	☒	Integrated text and data processing system - allows independent and simultaneous emulation of display and printer and provides for processing of link data before output	
15	US 4443864 A	☒	Memory for processor with multiplexed address - maps bus to memory device connections and internally connects unused pins to address inputs or data input-output lines	
16	DD 208254 A	☐	Interface for serial data transmission - is assigned simple priorities allowing large number of async. slave computers to be used remotely from master	

	Document ID	U	Title	Current OR
1	US 20030 23520 3 A1	☐	Extender sublayer device	370/445
2	US 20030 02882 9 A1	☒	Remote monitoring of computer devices	714/47
3	US 20020 04472 3 A1	☒	Optical signal processing device	385/24
4	US 65231 36 B1	☒	Semiconductor integrated circuit device with processor	714/30
5	US 61187 24 A	☒	Memory controller architecture	365/230 .05
6	US 60555 94 A	☒	Byte accessible memory interface using reduced memory control pin count	710/100
7	US 59699 97 A	☒	Narrow data width DRAM with low latency page-hit operations	365/189 .02
8	US 59481 14 A	☒	Integrated circuit binary data output interface for multiplexed output of internal binary information elements from input/output pads	714/733
9	US 58260 04 A	☒	Input/output device with self-test capability in an integrated circuit	714/25
10	US 57712 32 A	☒	Expandable local inter-system bus architecture in a multiplexed environment	370/384
11	US 56617 78 A	☒	Performance monitoring of DSO channel via D4 channel bank	379/29. 01
12	US 56551 33 A	☒	Massively multiplexed superscalar Harvard architecture computer	712/23
13	US 56174 31 A	☒	Method and apparatus to reuse existing test patterns to test a single integrated circuit containing previously existing cores	714/738
14	US 56131 44 A	☒	Serial register multi-input multiplexing architecture for multiple chip processor	712/43
15	US 54991 08 A	☒	Document-driven scanning input device communicating with a computer	358/400
16	US 54817 36 A	☒	Computer processing element having first and second functional units accessing shared memory output port on prioritized basis	712/23
17	US 54737 58 A	☒	System having input output pins shifting between programming mode and normal mode to program memory without dedicating input output pins for programming mode	711/103
18	US 54736 65 A	☒	Performance monitoring of DS0 channel via D4 channel bank	379/27. 01
19	US 51014 98 A	☒	Pin selectable multi-mode processor	710/316
20	US 49012 68 A	☒	Multiple function data processor	708/513
21	US 47207 83 A	☒	Peripheral bus with continuous real-time control	700/9
22	US 46758 41 A	☒	Micro computerized electronic postage meter system	705/402

	Document ID	U	Title	Current OR
23	US 4603385 A	☒	Integrated data processing/text processing system having a terminal with dual emulation and enhanced function capabilities	703/24
24	US 4425665 A	☒	FSK Voiceband modem using digital filters	375/223
25	US RE30331 E	☒	Data processing system having a unique CPU and memory timing relationship and data path configuration	711/105
26	US 4133028 A	☒	Data processing system having a CPU register file and a memory address register separate therefrom	710/104
27	US 4079454 A	☒	Data processing system using read-only-memory arrays to provide operation in a plurality of operating states	712/37
28	US 4075692 A	☒	Data path configuration for a data processing system	711/149
29	US 4017839 A	☒	Input/output multiplexer security system	710/51
30	US 4014006 A	☐	Data processing system having a unique CPU and memory tuning relationship and data path configuration	713/600

	Document ID	U	Title	Current OR
1	US 20030 22346 6 A1	☐	Apparatus for redundant multiplexing and remultiplexing of program streams and best effort data	370/537
2	US 20030 22262 5 A1	☒	CIRCUIT AND METHOD FOR POWER MEDIATION IN ELECTRONIC DEVICE	320/166
3	US 20030 22119 5 A1	☒	System for the transmission of audiovisual signals between source nodes and destination nodes	725/78
4	US 20030 18909 8 A1	☒	Planar light illumination and imaging (PLIIM) systems employing LED-based planar light illumination arrays (PLIAS) and linear electronic image detection arrays	235/454
5	US 20030 16303 4 A1	☒	Monitoring mayer wave effects based on a photoplethysmographic signal	600/372
6	US 20030 15091 7 A1	☒	Planar light illumination and imaging (PLIIM) system employing led-based planar light illumination arrays (PLIAS) and an area-type image detection array	235/454
7	US 20030 15091 6 A1	☒	LED-based planar light illumination and imaging (PLIIM) systems	235/454
8	US 20030 14966 2 A1	☒	Apparatus, systems and methods for wirelessly transacting financial transfers , electronically recordable authorization transfers, and other information transfers	705/39
9	US 20030 14628 2 A1	☒	Bioptical product and produce identification systems employing planar laser illumination and imaging (PLIM) based subsystems	235/454
10	US 20030 07449 8 A1	☒	Method and circuitry for a programmable controller system	710/36
11	US 20030 04230 8 A1	☒	Pliim-based semiconductor chips	235/454
12	US 20030 03926 3 A1	☒	Application module interface for a control channel in a private branch exchange (PBX) environment	370/422
13	US 20030 03720 0 A1	☒	Low-power reconfigurable hearing instrument	710/316
14	US 20030 03496 0 A1	☒	Coordinates input device and method for the same	345/179
15	US 20030 03495 9 A1	☒	One chip USB optical mouse sensor solution	345/166
16	US 20030 03086 2 A1	☒	Device and method for monitoring signal characteristics of optical signals in an optical communications network	398/5
17	US 20030 02115 7 A1	☒	Data line disturbance free memory block divided flash memory and microcomputer having flash memory therein	365/185 .33

	Document ID	U	Title	Current OR
18	US 20030014567 A1	☒	Personalized automated operator position	710/1
19	US 20030006289 A1	☒	Automated system and method for identifying and measuring packages transported through an omnidirectional laser scanning tunnel	235/470
20	US 20020196853 A1	☒	REDUCED RESOLUTION VIDEO DECOMPRESSION	375/240.16
21	US 20020195496 A1	☒	Planar LED-based illumination array (PLIA) chips	235/462.01
22	US 20020188181 A1	☒	Interface for a portable point-of-care patient diagnostic device	600/300
23	US 20020186233 A1	☒	Real time video production system and method	345/716
24	US 20020181289 A1	☒	Data line disturbance free memory block divided flash memory and microcomputer having flash memory therein	365/185.33
25	US 20020180627 A1	☒	Automatic A/D sample triggering	341/122
26	US 20020175931 A1	☒	Playlist for real time video production	345/716
27	US 20020172465 A1	☒	Fault-tolerant fiber-optical multiwavelength processor	385/47
28	US 20020153422 A1	☒	Planar led-based illumination modules	235/454
29	US 20020150061 A1	☒	Method and apparatus for performing satellite selection in a broadcast communication system	370/326
30	US 20020145394 A1	☒	Systems and methods for programming illumination devices	315/291
31	US 20020139853 A1	☒	Planar laser illumination and imaging (PLIIM) system employing wavefront control methods forreducing the power of speckle-pattern noise digital images acquired by said system	235/462.01
32	US 20020124104 A1	☒	Network element and a method for preventing a disorder of a sequence of data packets traversing the network	709/238
33	US 20020122228 A1	☒	Network and method for propagating data packets across a network	398/98
34	US 20020109710 A1	☒	Real time video production system and method	345/723

	Document ID	U	Title	Current OR
35	US 20020105553 A1	☒	Automated keyboard mouse switch	345/862
36	US 20020095515 A1	☒	Method and apparatus for identifying an I/O network in a process control system	709/245
37	US 20020061012 A1	☒	Cable modem with voice processing capability	370/352
38	US 20020051382 A1	☒	Data line disturbance free memory block divided flash memory and microcomputer having flash memory therein	365/185.08
39	US 20020048189 A1	☒	Data line disturbance free memory block divided flash memory and microcomputer having flash memory therein	365/185.08
40	US 20020043561 A1	☒	Method of and system for producing digital images of objects with subtantially reduced speckle-noise patterns by illuminating said objects with spatially and/or temporally coherent-reduced planar laser illumination	235/454
41	US 20020031756 A1	☒	Interactive tutorial method, system, and computer program product for real time media production	434/362
42	US 20020021289 A1	☒	Input device having two joysticks and touchpad with default template	345/173
43	US 20020018126 A1	☒	Image sensing apparatus, image processing apparatus and image sensing system	348/222.1
44	US 20020012143 A1	☒	Optical switch with connection verification	398/87
45	US 20010037508 A1	☒	Variable bandwidth communication systems and methods	725/105
46	US 20010033583 A1	☒	Voice gateway with downstream voice synchronization	370/503
47	US 20010030709 A1	☒	Method and apparatus for a digital parallel processor for film conversion	348/459
48	US 20010030690 A1	☒	Image detection processor	348/159
49	US 20010015912 A1	☒	Data line disturbance free memory block divided flash memory and microcomputer having flash memory therein	365/185.29
50	US 20010013793 A1	☒	Programmable logic device incorporating function blocks operable as wide-shallow ram	326/40
51	US 20010010467 A1	☒	Bioelectrical impedance measuring apparatus constructed by one-chip integrated circuit	324/601

	Document ID	U	Title	Current OR
52	US 6680601 B2	☒	Circuit and method for power mediation in electronic device	320/166
53	US 6654828 B2	☒	Personalized automated operator position	710/62
54	US 6651129 B1	☒	Apparatus and method for establishing a data communication interface to control and configure an electronic system with analog and digital circuits	710/316
55	US 6645820 B1	☒	Polycrystalline silicon diode string for ESD protection of different power supply connections	438/372
56	US 6636273 B1	☒	Remote control dedicated keybutton for confirming tuner setting of a TV set to a specific channel setting	348/734
57	US 6616048 B2	☒	Automated system and method for identifying and measuring packages transported through an omnidirectional laser scanning tunnel	235/472.02
58	US 6606483 B1	☒	Dual open and closed loop linear transmitter	455/126
59	US 6580953 B1	☒	Electrical control apparatus including retrievable stored operationing program	700/86
60	US RE38127 E	☒	Portable hybrid communication system and methods	455/557
61	US 6563799 B1	☒	Application module interface for hardware control signals in a private branch exchange (PBX) environment	370/264
62	US 6517004 B2	☒	Automated system for identifying and dimensioning packages transported through a laser scanning tunnel using laser scanning beam indexing techniques	235/472.02
63	US 6493271 B2	☒	Data line disturbance free memory block divided flash memory and microcomputer having flash memory therein	365/185.33
64	US 6472888 B2	☒	Bioelectrical impedance measuring apparatus constructed by one-chip integrated circuit	324/691
65	US 6452612 B1	☒	Real time video production system and method	345/723
66	US 6430165 B1	☒	Method and apparatus for performing satellite selection in a broadcast communication system	370/316
67	US 6414878 B2	☒	Data line disturbance free memory block divided flash memory and microcomputer having flash memory therein	365/185.33
68	US 6414746 B1	☒	3-D imaging multiple target laser radar	356/4.01
69	US 6407554 B1	☒	Diagnostic tester for electronic control devices in a variety of motor vehicle types	324/503
70	US 6400609 B1	☒	Data line disturbance free memory block divided flash memory and microcomputer having flash memory therein	365/185.28
71	US 6382515 B1	☒	Automated system and method for identifying and measuring packages transported through a laser scanning tunnel	235/472.01
72	US 6369855 B1	☒	Audio and video decoder circuit and system	348/423.1
73	US 6356626 B1	☒	Point to point voice message processor, method and recording/playback device	379/88.22
74	US 6356108 B2	☒	Programmable logic device incorporating function blocks operable as wide-shallow RAM	326/40

	Document ID	U	Title	Current OR
75	US 6335879 B1	☒	Method of erasing and programming a flash memory in a single-chip microcomputer having a processing unit and memory	365/185.08
76	US 6327342 B1	☒	E911 backup system for emergency 911 call answering systems	379/45
77	US 6324405 B1	☒	Communications apparatus and method for mobile platforms having a plurality of users	455/456.1
78	US 6310661 B1	☒	Method of broadcasting controlling data streams and apparatus for receiving the same	348/725
79	US 6304907 B1	☒	Network resource access method and apparatus	709/229
80	US 6301623 B1	☒	Computer network with a plurality of identically addressed devices	709/253
81	US 6292326 B1	☒	Disk device and removable magnetic disk device with electrically separated circuit portions for improved electro-magnetic compatibility	360/97.01
82	US 6292017 B1	☒	Programmable logic device incorporating function blocks operable as wide-shallow RAM	326/40
83	US 6282206 B1	☒	Variable bandwidth communication systems and methods	370/468
84	US 6278975 B1	☒	Voice command and control medical care system	704/275
85	US 6265987 B1	☒	Remote control device with learning function	340/825.69
86	US 6263396 B1	☒	Programmable interrupt controller with interrupt set/reset register and dynamically alterable interrupt mask for a single interrupt processor	710/263
87	US 6201737 B1	☒	Apparatus and method to characterize the threshold distribution in an NROM virtual ground array	365/185.16
88	US 6181598 B1	☒	Data line disturbance free memory block divided flash memory and microcomputer having flash memory	365/185.11
89	US 6173358 B1	☒	Computer system having dual bus architecture with audio/video/CD drive controller/coprocessor having integral bus arbitrator	711/100
90	US 6166953 A	☒	Data line disturbance free memory block divided flash memory and microcomputer having flash memory therein	365/185.11
91	US 6130836 A	☒	Semiconductor IC device having a control register for designating memory blocks for erasure	365/185.03
92	US 6122747 A	☒	Intelligent subsystem interface for modular hardware system	713/323
93	US 6122716 A	☒	System and method for authenticating a computer memory	711/163
94	US 6122687 A	☒	Multimedia computer system having multimedia bus	710/100
95	US 6116508 A	☒	Portable code reading and cursor pointing	235/462.13
96	US 6104208 A	☒	Programmable logic device incorporating function blocks operable as wide-shallow RAM	326/40
97	US 6097218 A	☒	Method and device for isolating noise sensitive circuitry from switching current noise on semiconductor substrate	326/82

	Document ID	U	Title	Current OR
98	US 6087930 A	☒	Active integrated circuit transponder and sensor apparatus for transmitting vehicle tire parameter data	340/447
99	US 6078465 A	☒	Disk device and removable magnetic disk device with electrically separated circuit portions for improved electro-magnetic compatibility	360/97.01
100	US 6067035 A	☒	Method for monitoring the operability of an analog to digital converter configured for digitizing analog signals	341/120
101	US 6064593 A	☒	Semiconductor integrated circuit device having an electrically erasable and programmable nonvolatile memory and a built-in processing unit	365/185.11
102	US 6034623 A	☒	Autonomous radio telemetry	340/870.01
103	US 6031343 A	☒	Bowling center lighting system	315/292
104	US 6026020 A	☒	Data line disturbance free memory block divided flash memory and microcomputer having flash memory therein	365/185.11
105	US 5978593 A	☒	Programmable logic controller computer system with micro field processor and programmable bus interface unit	710/1
106	US 5946634 A	☒	Mobile communications	455/552.1
107	US 5928340 A	☒	Apparatus for translating a bias signal into one of two different bias signals for a switching device	710/69
108	US 5918194 A	☒	Integrated modular measurement system having configurable firmware architecture and modular mechanical parts	702/91
109	US 5909595 A	☒	Method of controlling I/O routing by setting connecting context for utilizing I/O processing elements within a computer system to produce multimedia effects	710/38
110	US 5875311 A	☒	Computer system with touchpad support in operating system	710/305
111	US 5853244 A	☒	Intelligent system and process for automated monitoring of microingredient inventory used in the manufacture of medicated feed rations	366/141
112	US 5850265 A	☒	Intelligent television receiver and method of processing data therein	725/110
113	US 5838828 A	☒	Method and apparatus for motion estimation in a video signal	382/236
114	US 5815144 A	☒	Icon-based reset for cartridge memory computer system	345/717
115	US 5805138 A	☒	Gross motion input controller for a computer system	345/156
116	US 5802544 A	☒	Addressing multiple removable memory modules by remapping slot addresses	711/5
117	US 5768194 A	☒	Data line disturbance free memory block divided flash memory and microcomputer having flash memory therein	365/185.33
118	US 5765197 A	☒	Method and system for authentication of a memory unit for a computer system	711/164
119	US 5761698 A	☒	Computer system having audio/video/CD drive controller/coprocessor having integral memory interface, graphics coprocessor, digital signal processor, compact disk controller, and video controller	711/100

	Document ID	U	Title	Current OR
120	US 5736838 A	☒	High speed power factor controller	323/211
121	US 5731754 A	☒	Transponder and sensor apparatus for sensing and transmitting vehicle tire parameter data	340/447
122	US 5719862 A	☒	Packet-based dynamic de-skewing for network switch with local or central clock	370/355
123	US 5708436 A	☒	Multi-mode radar system having real-time ultra high resolution synthetic aperture radar (SAR) capability	342/25
124	US 5681220 A	☒	Keyboard touchpad combination in a bivalve enclosure	463/37
125	US 5666516 A	☒	Protected programmable memory cartridge having selective access circuitry	711/163
126	US 5627584 A	☒	Endoscope system with centralized control of associated peripheral equipment	348/72
127	US 5613137 A	☒	Computer system with touchpad support in operating system	710/1
128	US 5613069 A	☒	Non-blocking packet switching network with dynamic routing codes having incoming packets diverted and temporarily stored in processor inputs when network ouput is not available	709/238
129	US 5603043 A	☒	System for compiling algorithmic language source code for implementation in programmable hardware	712/1
130	US 5602750 A	☒	Administrative computer and testing apparatus	702/122
131	US 5602728 A	☒	Three button programmable sprinkler controller	700/16
132	US 5581503 A	☒	Data line disturbance free memory block divided flash memory and microcomputer having flash memory therein	365/185.33
133	US 5568138 A	☒	Servo-controlling system incorporated in keyboard instrument for processing parallel input signals in time sharing fashion	341/20
134	US 5534860 A	☒	Multiple key array	341/22
135	US 5487603 A	☒	Intelligent system and process for automated monitoring of microingredient inventory used in the manufacture of medicated feed rations	366/141
136	US 5483827 A	☒	Active integrated circuit transponder and sensor apparatus for sensing and transmitting vehicle tire parameter data	73/146.5
137	US 5477858 A	☒	Ultrasound blood flow/tissue imaging system	600/441
138	US 5477535 A	☒	Method of preventing a divergence of an adaptive echo canceller in a noisy signal environment	370/291
139	US 5471627 A	☒	Systolic array image processing system and method	712/19
140	US 5469045 A	☒	High speed power factor controller	323/211
141	US 5440311 A	☒	Complementary-sequence pulse radar with matched filtering and Doppler tolerant sidelobe suppression preceding Doppler filtering	342/132

	Document ID	U	Title	Current OR
142	US 5428806 A	☒	Computer networking system including central chassis with processor and input/output modules, remote transceivers, and communication links between the transceivers and input/output modules	710/104
143	US 5420921 A	☒	Method for the detection of a disable tone signal of an echo canceller	379/406.04
144	US 5396488 A	☒	Method for non-linear signal processing in an echo canceller	370/288
145	US 5327554 A	☒	Interactive terminal for the access of remote database information	725/110
146	US 5325500 A	☒	Parallel processing units on a substrate, each including a column of memory	711/157
147	US 5309564 A	☒	Apparatus for networking computers for multimedia applications	398/45
148	US 5303078 A	☒	Apparatus and method for large scale ATM switching	398/51
149	US 5257397 A	☒	Mobile data telephone	455/553.1
150	US 5253308 A	☒	Massively parallel digital image data processor using pixel-mapped input/output and relative indexed addressing	382/304
151	US 5216623 A	☒	System and method for monitoring and analyzing energy characteristics	702/62
152	US 5204861 A	☒	Key telephone system with enhanced connectivity	370/524
153	US 5184302 A	☒	Engine control apparatus including A/D converter failure detection element and method therefor	701/114
154	US 5169384 A	☒	Apparatus for facilitating post-traumatic, post-surgical, and/or post-inflammatory healing of tissue	604/20
155	US 5122735 A	☒	Digital power metering	324/142
156	US 5115358 A	☒	Configurable disk memory servowriter	360/75
157	US 5076060 A	☒	Sensible body vibration	601/59
158	US 4970721 A	☒	Resource-decoupled architecture for a telecommunications switching system	370/355
159	US 4967340 A	☒	Adaptive processing system having an array of individually configurable processing components	712/19
160	US 4958182 A	☒	Arrangement for determining camera setting	396/292
161	US 4937527 A	☒	Lead assembly for a distributorless ignition interface	324/402
162	US 4928258 A	☒	Recursive median filtering	708/320
163	US 4907556 A	☒	Electronic control system for internal combustion engine	123/486

	Document ID	U	Title	Current OR
164	US 4870564 A	☒	Distributed input/output system	710/12
165	US 4858107 A	☒	Computer device display system using conditionally asynchronous memory accessing by video display controller	711/158
166	US 4849780 A	☒	Information setting device for camera	396/297
167	US 4847563 A	☒	Distributorless ignition interface	324/402
168	US 4788531 A	☒	Automatic fault reporting system	340/945
169	US 4764868 A	☒	Distributed input/output system	710/12
170	US H000481 H	☒	Microprocessor controlled RF modulator apparatus	342/170
171	US 4719459 A	☒	Signal distribution system switching module	340/2.27
172	US 4701870 A	☒	Integrated circuit device testable by an external computer system	702/120
173	US 4675675 A	☒	Automatic fault reporting system	340/945
174	US 4661692 A	☒	Microscope provided with automatic focusing device having memory means	250/201.2
175	US 4647195 A	☒	Automotive headlamp testing method and apparatus	356/121
176	US 4643540 A	☒	Microscope provided with an automatically controlled illuminating optical system	359/368
177	US 4639783 A	☒	Video signal field/frame storage system	348/446
178	US 4638452 A	☒	Programmable controller with dynamically altered programmable real time interrupt interval	710/266
179	US 4633750 A	☒	Key-touch value control device of electronic key-type musical instrument	84/626
180	US 4593237 A	☒	Servo-system having an adjustment indicator	318/561
181	US 4573057 A	☒	Continuous ink jet auxiliary droplet catcher and method	347/74
182	US 4571049 A	☒	Photographic camera of multiple spot photometry type	396/213
183	US 4535453 A	☒	Signaling input/output processing module for a telecommunication system	370/384
184	US 4529289 A	☒	Camera	396/233
185	US 4517637 A	☒	Distributed measurement and control system for industrial processes	700/9
186	US 4510840 A	☒	Musical note display device	84/477R

	Document ID	U	Title	Current OR
187	US 4506377 A	☒	Spoken-instruction controlled system for an automotive vehicle	704/275
188	US 4497031 A	☒	Direct digital control apparatus for automated monitoring and control of building systems	700/276
189	US 4482961 A	☒	Automatic control system for directional control of an aircraft during landing rollout	701/16
190	US 4471424 A	☒	Apparatus and method for conditioning grain	700/16
191	US 4468614 A	☒	Average frequency measuring apparatus	324/76.58
192	US RE31651 E	☒	Communication system using intelligent network processor	370/383
193	US 4442502 A	☒	Digital information switching system	710/316
194	US 4407290 A	☒	Blood constituent measuring device and method	600/330
195	US 4387365 A	☒	Real time digital scan converter	708/442
196	US 4360769 A	☒	Optical counting motor shaft positioner	318/601
197	US 4357849 A	☒	Key switch information assignor	84/617
198	US 4354576 A	☒	Command speed generator system for elevator car	187/293
199	US 4193116 A	☒	Analysis instrument	702/23
200	US 4117364 A	☐	Voltage waveform synthesizer and a system that includes the same	318/810

	L #	Hits	Search Text	DBs
1	L1	183073	((i adj1 o) input$4 output$4) near20 (port pin pad)	USPAT; US-PGPUB
2	L2	13897	1 near50 ((select$5 reconfigur$4 configur$4) near20 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
3	L3	769	2 near50 ((process$3 core internal$2 inside (on adj1 chip)) near20 (resource element unit module device peripher$2))	USPAT; US-PGPUB
4	L4	11402	1 near20 ((select$5 reconfigur$4 configur$4) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
5	L5	452	4 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	USPAT; US-PGPUB
6	L7	21135	1 near20 ((select$5 reconfigur$4 configur$4 switch$3) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
7	L9	908	7 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	USPAT; US-PGPUB
8	L10	631	(pin port pad (i adj1 o) input$4 out$4).ab,ti. and 9	USPAT; US-PGPUB
9	L12	71320	((i adj1 o) input$4 output$4) near20 (port pin pad)	EPO; JPO; DERWENT; IBM_TDB
10	L16	4471	12 near20 ((select$5 reconfigur$4 configur$4 switch$3) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	EPO; JPO; DERWENT; IBM_TDB
11	L11	397	(pin port pad).ab,ti. and 9	USPAT; US-PGPUB
12	L17	158	16 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	JP 2003084919 A	☐	CONTROL METHOD OF DISK ARRAY DEVICE, AND DISK ARRAY DEVICE	
2	JP 2002342253 A	☒	METHOD FOR CONTROLLING STORAGE SUB-SYSTEM AND STORAGE SUB-SYSTEM	
3	JP 2002323968 A	☒	MULTICOMPUTER SYSTEM	
4	JP 2001285347 A	☒	DEVICE FOR PACKET SWITCHING AND METHOD FOR STATISTICS INFORMATION PROCESSING	
5	JP 2001223793 A	☒	MESSAGE TRANSFER PART LEVEL-3 ALIAS POINT CODE	
6	JP 2001156257 A	☒	SEMICONDUCTOR INTEGRATED CIRCUIT	
7	JP 2001133511 A	☒	SEMICONDUCTOR DEVICE	
8	JP 2001007847 A	☒	MULTI-PROTOCOL PROCESSING DEVICE, CIRCUIT INTERFACE AND MULTI-PROTOCOL SWITCH SYSTEM HAVING THEM	
9	JP 2000330879 A	☒	METHOD AND DEVICE FOR TESTING INPUT/OUTPUT CHANNEL	
10	JP 2000231535 A	☒	DATA PROCESSOR HAVING MEMORY COUPLING UNIT	
11	JP 2000069004 A	☒	FLOW CONTROL METHOD FOR EXCHANGE SYSTEM AND EXCHANGE SYSTEM	
12	JP 11306132 A	☒	METHOD AND PROCESSOR FOR SIGNAL PROCESSING AND DIGITAL BROADCAST RECEIVING DEVICE	
13	JP 10215259 A	☒	SWITCH FOR PACKET COMMUNICATION SYSTEM	
14	JP 09217534 A	☒	AUTOMATIC LOCKING DEVICE FOR VEHICULAR KEYLESS SYSTEM	
15	JP 08278839 A	☒	CONNECTION SWITCHING DEVICE	
16	JP 08204544 A	☒	PROGRAMMABLE LOGIC CIRCUIT ELEMENT	
17	JP 08137819 A	☒	CONNECTION CONTROLLER	
18	JP 08006737 A	☒	FAULT RESISTANT DATA STORAGE SUB-SYSTEM AND DATA PROCESSING SYSTEM	
19	JP 07191947 A	☒	PARALLEL COMPUTERS	

	Document ID	U	Title	Current OR
20	JP 07047 878 A	☒	HEADLAMP FOR VEHICLE	
21	JP 06314 264 A	☒	SELF-ROUTING CROSS BAR SWITCH	
22	JP 05128 721 A	☒	MAGNETIC RECORDING AND REPRODUCING DEVICE	
23	JP 05027 864 A	☒	POWER FAILURE COMPENSATING STRUCTURE FOR MICROCOMPUTER EQUIPMENT	
24	JP 04295 954 A	☒	DATA PROCESSOR	
25	JP 04291 179 A	☒	DC TEST SYSTEM FOR INPUT AND OUTPUT BUFFERS OF INTEGRATED CIRCUIT	
26	JP 04238 588 A	☒	SINGLE CHIP MICROCOMPUTER	
27	JP 04169 982 A	☒	MICROCOMPUTER	
28	JP 04068 554 A	☒	SEMICONDUCTOR INTEGRATED CIRCUIT	
29	JP 04056 150 A	☒	LARGE SCALE INTEGRATED CIRCUIT	
30	JP 04023 445 A	☒	SPECIFYING METHOD OF REFLECTION NOISE GENERATING PIN	
31	JP 03161 854 A	☒	SERIAL PORT CONTROL SYSTEM	
32	JP 03110 660 A	☒	MULTIPORT SWITCHING CONTROL SYSTEM	
33	JP 03081 823 A	☒	PERSONAL COMPUTER	
34	JP 02239 357 A	☒	COMPUTER INTERFACE	
35	JP 02186 661 A	☒	INTEGRATED CIRCUIT	
36	JP 01125 646 A	☒	INFORMATION PROCESSOR	
37	JP 62219 054 A	☒	SYSTEM FOR CONNECTING I/O PORT DEVICES	
38	JP 61223 669 A	☒	LSI TEST SYSTEM	
39	JP 61122 038 A	☒	GEAR PARKING APPARATUS OF VEHICLE	
40	JP 58076 910 A	☒	ABNORMAL STATE DETECTING DEVICE	
41	JP 56031 813 A	☒	AIR CONDITIONER FOR VEHICLE	
42	JP 54079 041 A	☒	CONTROL METHOD FOR COPIER	

	Document ID	U	Title	Current OR
43	EP 1186969 A2	☒	Alarm clock with remote control function	
44	EP 1094382 A1	☒	Reset device and control system	
45	EP 1001648 A2	☒	Switch architecture for digital multiplexed signals	
46	EP 878938 A2	☒	System for conducting rate control of ATM traffic	
47	EP 689143 A1	☒	Data storage subsystem	
48	EP 632660 A1	☒	Monitor system with automatic recording control.	
49	EP 623880 A2	☒	Crossbar switch for multiprocessor system.	
50	EP 550187 A2	☒	Analog to digital converter calibration system and method of operation.	
51	EP 511834 A2	☒	Multi-stage interconnect network for processing system.	
52	EP 347929 A2	☒	Parallel processor.	
53	DE 3716141 A1	☒	Charge indicator for ISDN switching systems	
54	EP 282227 A1	☒	Signal switching processor.	
55	US 20030144024 A	☒	Multiple telephone numbers provision apparatus for cellular telephone, has central processing unit with input ports connected to cellular telephone, to receive reset signal so as to control switching of telephone numbers	
56	CA 2369178 A	☒	Crossbar switching fabric for data routing has multiple crossbar ingress and egress processing units with memory buffer for data storage	
57	KR 20030033339 A	☒	Device for recognizing multi-signal and method thereof	
58	WO 2003050640 A	☒	Data processor for architectures of high-performance parallel computing systems has functional units and switchboard to selectively connect the input operand ports of functional units to result ports of each of other functional units	
59	US 20030065858 A	☒	Input apparatus e.g. keyboard for handheld information processor, includes route selection unit which disconnects/connects transmission route between main and transmission connection ports based on logic level	
60	US 20030056565 A	☒	Chemical dispensing system for washing machine, has sensors which outputs signal corresponding to quantity of liquid chemical in respective chemical pod	
61	US 20030058873 A	☒	Network device such as network processor based multi-port switch has parallel compression/decompression engine coupled to memory buffer which is configured as data cache to input data to processor	
62	KR 20030010859 A	☒	Performance extendable clos switching system	

	Document ID	U	Title	Current OR
63	US 20030 04646 0 A	☒	Controlling method for disk array system involves temporarily holding large number of packets, received from one of two interface units communicating with host system and disk drives, in switch unit	
64	JP 20030 29919 A	☒	Input device for portable computers, switches its operation mode, when connected/disconnected from information processor	
65	US 20020 18643 4 A	☒	Communication channel routing method for optical communication network, involves allocating wavelength selective element of internal route connecting input and output ports of transparent photonic switch	
66	US 20020 14391 0 A	☒	Network hub for controlling connection between server and workstations in LAN, has switching circuits to control conduction or cut-off of connecting ports based on control signals output by signal processing circuit	
67	US 20020 08330 8 A	☒	Data processing device has configurable connection circuits to pass operand and result bits between input and output ports of configurable functional unit through configurable logic blocks	
68	JP 20021 64849 A	☒	Wavelength division multiplexing transmission device for optical network, has switch control circuit to control matrix switch which connects input-output ports and optical transmitting and receiving modules	
69	KR 20020 25525 A	☒	Method of utilizing virtual path identifier and virtual channel identifier of internal switching cell in asynchronous transfer mode switching system	
70	DE 10036 643 A	☒	Method and device for controlling operating routines in motor vehicle engine control uses a processor module to link to a bus system like a select port interface bus via a bus input/output interface while communicating through it.	
71	WO 20021 0930 A	☒	Multiprocessor system with several processor modules coupled together via backplane has switch with I/O ports for routing Ethernet MAC protocol data packets from one of first, second and third processors to another of the three processors	
72	JP 20020 26749 A	☒	Digital-signal processing apparatus for radio connected to PC, has input-output port of arbitrary submodule selected from submodules having signal-processing circuits, that is connected to input-output port of main module	
73	WO 20018 3007 A	☒	Closed loop system for controlling administration of medication to patient, comprises sensor package, medication delivery unit, and medication delivery controller	
74	US 63113 03 B	☒	Integrated circuit debugging method uses circuit modules to drive otherwise inaccessible internal signals through monitor port and has trace select register to enable selected modules	
75	WO 20017 9979 A	☒	Navigation control unit for a wireless communication resource access device using a microprocessor to store information regarding the control unit and to process user input	
76	US 62694 58 B	☒	Fault diagnosing and isolating method in computer system, involves comparing two values from different memory areas, by processor which indicates error when values are different	
77	KR 20010 64227 A	☒	Interface method of network processing module in multilayer packet switch system and multilayer packet switch system thereof	
78	KR 20010 56947 A	☒	Interface between cpu and dsp in cdma mobile communication system	
79	JP 20010 69196 A	☒	Multifunctional processing apparatus for vehicle navigation apparatus, switches processing of signals input to common and different pins of interface section based on communication mode of devices recognized	
80	US 61608 11 A	☒	Data packet router for providing communication between computer system, has input for interface modules to select processes for each packet based on data in respective packet header	

	Document ID	U	Title	Current OR
81	DE 19924 343 A	☒	Port control unit for program controlled device with input and output connections - with port control unit consisting of identical control modules and connected over common interface with internal bus of device and selected or configured according to temperature of device	
82	US 60492 25 A	☒	Programmable logic array device provides multiple levels of switching between interconnection conductors and output pins of programmable logic core	
83	WO 20000 4741 A	☒	Composite ATM switch configuration for ATM network	
84	JP 20000 20413 A	☒	Operation verification system for dynamic switch device used in input-output processor of host system - uses input-output simulators, which connect to dynamic switch ports of dynamic switch device, in input-output device side of host system to secure predetermined synchronization	
85	US 59599 94 A	☒	Enhanced asynchronous transfer mode switch for ATM cell traffic	
86	US 59562 80 A	☒	Contact test system for verifying contact between pins of memory tester and input-output I/O pins of a CMOS IC chip or module	
87	JP 11177 599 A	☒	Ethernet repeater for interconnection of several local area network terminals - connects port with large communication data with respective internal bus, when amount detector detects large amount of communication data in that port	
88	RU 21288 87 C	☒	Multifunctional telephone set	
89	RD 41709 7 A	☒	Interconnecting structure between N ports switch module and backplane connector - has peripheral zone which is boundary between internal wiring and external wiring where internal wiring connects channels to input/output terminals of module	
90	US 59387 36 A	☒	Search engine architecture for computer network multi-layer switch element - configured to schedule and perform accesses to forwarding memory and to transfer forwarding decisions to input ports	
91	US 58322 91 A	☒	Interconnection architecture between processor array, external memory and input-output port - has memory channels comprising three single ported RAM corresponding to respective controller channels	
92	JP 10275 141 A	☒	Calculating device used for e.g. communication data processing operation of network apparatus - has MPX and DMPX, connected to each input port and output port respectively, that selectively inputs and outputs several data from virtual node processor respectively	
93	US 58071 75 A	☒	OS reconfiguration method during connection or disconnection of player actuated digital input devices from computer port - involves processing input signal received from digital input device through port, without need for rebooting computer based on identified input device type	
94	JP 10207 831 A	☒	Priority level determination system for parallel processor connected to network - has sequential and non-sequential priority level determination units that select output port from ports that are to be sequentially assigned and need not be assigned to input port respectively	
95	WO 98321 12 A	☒	Sensory communication appts. e.g. for use by blind people - includes central processing unit with data store, controller for output of data from store to output processor and output element with tactile sensor units connected to receive data from processor so output can be determined by touch	
96	JP 10143 465 A	☒	Data forwarding system for information processors such as personal computer, workstation, server machine, office computer, mainframe, super computer - has large-scale -integrators connected to slice obtained by dividing data forwarding path of n-bit width by slice of m-bit width	

	Document ID	U	Title	Current OR
97	US 5751764 A	☒	Switch configuring method for TV post production facility - disabling ports to which two ports to be connected are currently connected, and configuring switching core to forward and reverse connections between the two ports	
98	US 5726985 A	☒	Asynchronous transfer mode communication system for processing and organising digital information - has I/O port interface that issues respective request for access to memory, programmable processor exercises executive control over pre-configured processor and input/output port interface device	
99	US 5719862 A	☒	Network switch with local or central clock - has temporary connection between input and output ports, with several media access controller modules having source and destination modules for receiving and transmitting data packets, with packet framer adding start flag	
100	JP 09304797 A	☒	Optical switch unit for optical signal processor, light transmitting system - has optical gate switch connected to each output port of optical switch element which switches with optical heating effect	
101	JP 09282900 A	☒	Memory module with various memory devices e.g. DRAM, SRAM for e.g. personal computer, workstation - has jumper chip that switches connection between input-output terminal and data input-output terminal of memory device and connects only input-output terminal with normal bit to data input-output terminal	
102	US 5657291 A	☒	Multiport register file memory array device for floating point processing unit - has several select and priority circuits having port inputs and outputs, output of select and priority circuit being connected to word line	
103	US 5999527 A	☒	Modular ATM switch for high rate transfer of data - has inputs for switch core units in each row connected to port in individual group and outputs of units in each column connected to port in same order group	
104	US' 5652900 A	☒	2n-bits width data bus for context switching function in data processor - has control unit is coupled to output port, instruction decoding unit and generates control signals to control execution of instructions according to output of instruction decoding unit	
105	US 5602750 A	☒	Administrative and testing appts for testing industrial equipment e.g computer - has instrumentation processor that control controllable relay switches in response to serial data signals received over serial port from administrative computer	
106	US 5602728 A	☒	Three button microprocessor-based programmable irrigation sprinkler valve control module - includes irrigation control processor mounted in controller housing and interfacable with personal computer, LCD display, menu cycle switch for cycling among menus of control program and output port connected to sprinkler valve	
107	JP 08329232 A	☒	Image data memory device for e.g. personal computer, word processor - has input and output switches which selectively performs data write-in operation through input port that is connected to transmitter or data read-out operation through output port that is connected to image processor	
108	JP 08278839 A	☒	Connection switching appts. for e.g. personal computer - has switch which connects several external device I-O ports to computer port through several connection switch I-O port based on detected data of data sensor of personal computer	
109	TW 283804 A	☒	Serial address generator for burst mode memory device - has internal and external address enable switches, and address arranging device with time burst input port, preset port and output port	
110	EP 726532 A	☒	Single instruction, multiple data processing system - has processor elements connected in cluster by common instruction bus to instruction memory	
111	GB 2296621 A	☒	Switch adaptor for ATM switch - has switch unit with several input and output ports, controller connected between specific input port and output port to control data process, and interface unit coupled to controller	

	Document ID	U	Title	Current OR
112	JP 08171 536 A	☒	High-speed data processor for e.g. image processing - has start timing delay unit which combines and delays start timing operation of each data processing unit, and several data bus connection switches connected to several data bus	
113	US 55328 44 A	☒	System for interfacing processor with image scanner - Has interface unit with switching device responsive to designated transfer mode to select either processor input ports or output ports	
114	JP 08064 648 A	☒	Semiconductor wafer for LSI mfg process - has decoding unit that is connected to pad and IC chip, which decodes chip selecting signal input from pad for probe contact	
115	EP 70000 3 A	☒	Data processor with controlled burst memory accesses - includes external bus interface circuit responsive to two internal bus master devices to perform either fixed or variable burst access	
116	GB 22917 70 A	☒	Display appts. for communicating control data via channel to computer system - includes user control panel with manually operable switches mounted in front of display unit for selectively connecting key=pad interrupt lines of processor to serial channel of cable via communication interface circuit and input unit	
117	EP 68914 3 A	☒	Fault tolerant data storage subsystem - has several storage device controllers emulating storage devices with cache memories with multiple data input=output ports and processing element to selectively interconnect selected input with output port in cache	
118	US 54778 58 A	☒	Ultrasound blood flow and tissue imaging system - has ultrasound coupling wedge to position transducer elements at fixed predetermined angle wrt skin of patient, and processor connected to output ports of switch to receive transducer outputs	
119	EP 79654 6 B	☒	Large capacity ATM switch - includes space switch core connecting input buffer modules and output buffer modules by high speed links and sends data in bursts consisting of ATM cell train	
120	US 55862 89 A	☒	Parallel computer with dedicated-storage access - has parallel computing architecture in which each processor has associated dedicated local memory which can be independently and asynchronously accessed by other processors	
121	US 57402 35 A	☒	User programmable paging system control appts. - includes multiple input devices providing access to paging system with multiple output options with higher priority access input always given priority over lower priority access input	
122	FR 27121 17 A	☒	Remote control function switching device for PC - has two segments with contacts and rocking about an axis being mounted on DIP switch while control unit transmits function switching signals and receives operation confirmation	
123	KR 95037 22 B	☒	Automatic calling circuit from inner subscriber to outer one in private telephone exchange - detects voice source in constant time interval	
124	EP 62401 7 A	☒	Packet data communication network with centralised management plane - enables management unit to be kept informed of network configuration and states of micro-nodes available for re-routing	
125	EP 62388 0 A	☒	Self routing crossbar switch for multiprocessor system - interconnects several processors with memory modules using self routing crossbar switch connecting processors and memory modules, with processor connected to each input port and memory to each output port	
126	US 54577 85 A	☒	Device-driver-software-transparent bus interface - uses master state-translation and controller to enable computer system to drive external I=O devices	
127	EP 59973 5 A	☒	Async. transfer mode data cell processing circuit for wideband communication network - has first-in-first-out memory with dual outputs separating header and information fields under control of reading input controls	
128	US 53172 10 A	☒	Input output cell for programmable logic device - has I/O pad directly connected with selected logic array block without travelling through latch of cell and internal bus of programmable logic device	

	Document ID	U	Title	Current OR
129	GB 2271897 A	☒	Electronic solid-state data processing device, e.g. for heating controller - uses bi-stable relay to select connection between port and line, to link devices, and to carry functionally different signals	
130	KR 9403028 B	☒	Function failure notifying device for voice processing system - comprises automatic switching circuit which connects tip port and ring port with message sending circuit if output power is down	
131	EP 657046 B	☒	Communications port for three port fault tolerant operation - has command protocol on parallel lines requiring computer to issue two complementary commands to complete inter processor communication	
132	JP 05316135 A	☒	Dual ring multi-state reconfiguration and access unit for serial communication network - has input and output for connecting primary and secondary rings of dual network, adaptors for receiving and re-transmitting signals and ports for attaching data terminals	
133	EP 562613 A	☒	Semicustom integrated circuit e.g. ECL gate array - has power source lines formed on peripheral circuit cells to surround internal circuit	
134	GB 2261967 A	☒	System status maintaining and supporting appts. - has console commonly connected to CPU and support processor to remotely monitor system status via I=O ports of support processor	
135	GB 2258925 A	☒	Semiconductor memory power voltage generator - has voltage sense and circuit reference voltage controller, both governing internal power voltage generator to provide internal voltage w.r.t. sensed level	
136	EP 506224 A	☒	Packaging structures for high performance computer system - supports very fast cycle time and high bandwidth by stacking ECMs with input output pads on three edges which support multiple processors per module	
137	US 5123011 A	☒	Modular multistage switch for parallel computing system - has identical modules which include on-board interconnections between input and output ports for providing interconnections among processors coupled to module	
138	EP 481645 A	☒	Test equipment for colour image processing appts. - supplies output of image processor to raster store for selective display or electronic comparison	
139	EP 535050 B	☒	Switching element for high speed data traffic - transmits data in parallel form between two input and two output ports using switching unit and control unit	
140	EP 422965 A	☒	Video signals circuit for continuous vector processor - has data transfer controller connected to input register set to enabling data transfer between registers	
141	GB 2229557 A	☒	Accessing addressable memory with reduced number of connections - setting start address in response to reset signal and altering it with clock signals	
142	US 4924426 A	☒	Selection circuitry fr distributing data blocks from external memory - has selector directly coupled to memory for receiving each data block read out from memory	
143	US 4847751 A	☒	Multi-task execution control system - has multi-task support processor controlling switching and communications between tasks under direction of received command	
144	EP 346420 B	☒	Multi-processor system for fast data exchange - uses series connections between memory and processor shift registers for transfer of data blocks	
145	EP 298845 A	☒	Interfering station suppression in switched radio direction finder - having AGC of each channel amplifier held fixed during each switching cycle by use of PIN diodes	
146	EP 289189 A	☒	Portable communications network hub device - serves as communications net for computers and answers to protocol requirements of adaptor cards	
147	SU 1425685 A	☒	Program debugging unit - sets several debugging modes in format of oje command byte with direct access memory modification	
148	EP 282825 A	☒	Digital signal processor e.g. for speech signals - has parallel data input-output ports which implement parallel communication independently of input-output operations and asynchronously	

	Document ID	U	Title	Current OR
149	EP 282227 A	☒	Signal switching processor esp. for optical signals - has input ports connected in pairs toto exchange-by=pass modules of group having ports coupled to redistribution network	
150	DE 3801869 A	☒	Digital signal processing for communication telephone system - has main controller which dynamically allocates circuit switch and message channels of programmable digital switch	
151	EP 272847 A	☒	bidirectional semiconductor device e.g. for use with FIFO memory - controls switches between internal and external parts by mode signal for bidirectional data transmission	
152	AU 8777673 A	☒	Distributed fault tolerant on-line transaction processing system - has internal bus connecting real time processor, applications program processor, local memory and one I=O processor	
153	CA 1182928 A	☒	Switchable element matrix scanning for microprocessor keyboard - using control and shift leads for state change of element and connecting logic gate to 2 output leads	
154	EP 104802 A	☒	Multiport module for async. speed independent processor network - has input selector circuit for each port to specify which output circuit connected to ports will transmit message	
155	EP 99978 A	☒	Star-loop communication system for processors and terminals - uses digital switch to set up loop-star or multi-drop configurations with monitor for switch connections	
156	EP 57511 A	☒	Information processing appts. for multiprocessor system - uses common port control circuit whether processor is master or slave	
157	US 4276451 A	☒	Fault monitoring and diagnostic system for switching system - uses test call generator to initiate tests and to re-route output signals using programmable switch if fault discovered	
158	WO 8000381 A	☐	Plug-in input and output simulator module - has switches assigned to connector pins to pass selected logic signal to processor unit of controller	

	L #	Hits	Search Text	DBs
1	L1	183073	((i adj1 o) input$4 output$4) near20 (port pin pad)	USPAT; US-PGPUB
2	L2	13897	1 near50 ((select$5 reconfigur$4 configur$4) near20 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
3	L3	769	2 near50 ((process$3 core internal$2 inside (on adj1 chip)) near20 (resource element unit module device peripher$2))	USPAT; US-PGPUB
4	L4	11402	1 near20 ((select$5 reconfigur$4 configur$4) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
5	L5	452	4 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	USPAT; US-PGPUB
6	L7	21135	1 near20 ((select$5 reconfigur$4 configur$4 switch$3) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
7	L9	908	7 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	USPAT; US-PGPUB
8	L10	631	(pin port pad (i adj1 o) input$4 out$4).ab,ti. and 9	USPAT; US-PGPUB
9	L12	71320	((i adj1 o) input$4 output$4) near20 (port pin pad)	EPO; JPO; DERWENT; IBM_TDB
10	L16	4471	12 near20 ((select$5 reconfigur$4 configur$4 switch$3) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	EPO; JPO; DERWENT; IBM_TDB
11	L11	397	(pin port pad).ab,ti. and 9	USPAT; US-PGPUB
12	L18	198	11 and @pd<20000906	USPAT; US-PGPUB
13	L17	158	16 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	EPO; JPO; DERWENT; IBM_TDB

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2	L2	13897	1 near50 ((select$5 reconfigur$4 configur$4) near20 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
3	L3	769	2 near50 ((process$3 core internal$2 inside (on adj1 chip)) near20 (resource element unit module device peripher$2))	USPAT; US-PGPUB
4	L4	11402	1 near20 ((select$5 reconfigur$4 configur$4) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
5	L5	452	4 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	USPAT; US-PGPUB
6	L7	21135	1 near20 ((select$5 reconfigur$4 configur$4 switch$3) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
7	L9	908	7 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	USPAT; US-PGPUB
8	L10	631	(pin port pad (i adj1 o) input$4 out$4).ab,ti. and 9	USPAT; US-PGPUB
9	L12	71320	((i adj1 o) input$4 output$4) near20 (port pin pad)	EPO; JPO; DERWENT; IBM_TDB
10	L16	4471	12 near20 ((select$5 reconfigur$4 configur$4 switch$3) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	EPO; JPO; DERWENT; IBM_TDB
11	L11	397	(pin port pad).ab,ti. and 9	USPAT; US-PGPUB
12	L17	158	16 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	EPO; JPO; DERWENT; IBM_TDB

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2	L2	13897	1 near50 ((select$5 reconfigur$4 configur$4) near20 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
3	L3	769	2 near50 ((process$3 core internal$2 inside (on adj1 chip)) near20 (resource element unit module device peripher$2))	USPAT; US-PGPUB
4	L4	11402	1 near20 ((select$5 reconfigur$4 configur$4) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
5	L5	452	4 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	USPAT; US-PGPUB
6	L7	21135	1 near20 ((select$5 reconfigur$4 configur$4 switch$3) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
7	L9	908	7 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	USPAT; US-PGPUB
8	L10	631	(pin port pad (i adj1 o) input$4 out$4).ab,ti. and 9	USPAT; US-PGPUB
9	L12	71320	((i adj1 o) input$4 output$4) near20 (port pin pad)	EPO; JPO; DERWENT; IBM_TDB
10	L16	4471	12 near20 ((select$5 reconfigur$4 configur$4 switch$3) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	EPO; JPO; DERWENT; IBM_TDB
11	L11	397	(pin port pad).ab,ti. and 9	USPAT; US-PGPUB
12	L17	158	16 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	EPO; JPO; DERWENT; IBM_TDB
13	L19	4902	12 near20 ((select$5 reconfigur$4 configur$4 switch$4 multiplex$3) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	EPO; JPO; DERWENT; IBM_TDB
14	L21	23497	1 near20 ((select$5 reconfigur$4 configur$4 switch$4 multiplex$3) near10 (interfac$3 connect$3 interconnect$3 coupl$3))	USPAT; US-PGPUB
15	L22	1033	21 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2))	USPAT; US-PGPUB
16	L24	292	22 and analog	USPAT; US-PGPUB
17	L20	16	19 near20 ((process$3 core internal$2 inside (on adj1 chip)) near10 (resource element unit module device peripher$2)) not 17	EPO; JPO; DERWENT; IBM_TDB
18	L23	30	(pin port pad).ab,ti. and 22 not 11	USPAT; US-PGPUB
19	L25	202	24 not (11 23)	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 6114848 A	☐	Direct-measurement provision of safe backdrive levels	324/158.1
2	US 6108725 A	☒	Multi-port internally cached DRAM system utilizing independent serial interfaces and buffers arbitratively connected under a dynamic configuration to allow access to a common internal bus	710/56
3	US 6105007 A	☒	Automatic financial account processing system	705/38
4	US 6104589 A	☒	Method of protecting an integrated circuit, method of operating integrated circuitry, and method of operating cascode circuitry	361/111
5	US 6104588 A	☒	Low noise electrostatic discharge protection circuit for mixed signal CMOS integrated circuits	361/111
6	US 6100670 A	☒	Multi-functional battery management module operable in a charging mode and a battery pack mode	320/150
7	US 6085090 A	☒	Autonomous interrogatable information and position device	455/440
8	US RE36751 E	☒	ATM switching system connectable to I/O links having different transmission rates	370/378
9	US 6081473 A	☒	FPGA integrated circuit having embedded sram memory blocks each with statically and dynamically controllable read mode	365/230.01
10	US 6075788 A	☒	Sonet physical layer device having ATM and PPP interfaces	370/395.51
11	US 6064679 A	☒	Hub port without jitter transfer	370/513
12	US 6064093 A	☒	Protection circuit with clamping feature for semiconductor device	257/355
13	US 6061345 A	☒	Crossbar routing switch for a hierarchical crossbar interconnection network	370/351
14	US 6061156 A	☒	Optical transmission system	398/55
15	US 6055235 A	☒	Switching system	370/389
16	US 6049225 A	☒	Input/output interface circuitry for programmable logic array integrated circuit devices	326/41
17	US 6049224 A	☒	Programmable logic device with logic cells having a flexible input structure	326/41
18	US 6044425 A	☒	Information processing system for selectively connecting multiple types of extension devices to connection ports	710/104
19	US 6035414 A	☒	Reliability of crossbar switches in an information processing system	714/7
20	US 6032204 A	☒	Microcontroller with a synchronous serial interface and a two-channel DMA unit configured together for providing DMA requests to the first and second DMA channel	710/23
21	US 6018518 A	☒	Flow control in a cell switched communication system	370/235
22	US 6016317 A	☒	ATM cell switching system	370/391

	Document ID	U	Title	Current OR
23	US 6014715 A	☒	Method and apparatus for assigning port addresses	710/11
24	US 6011791 A	☒	Multi-processor system and its network	370/352
25	US 6005867 A	☒	Time-division channel arrangement	370/409
26	US 5990577 A	☒	Hub for local area network with backup power supply system	307/26
27	US 5983377 A	☒	System and circuit for ASIC pin fault testing	714/726
28	US 5983291 A	☒	System for storing each of streams of data bits corresponding from a separator thereby allowing an input port accommodating plurality of data frame sub-functions concurrently	710/52
29	US 5983014 A	☒	Power management system that one of plurality of peripheral signals is selectably routed to main pad clock node during a test mode	702/60
30	US 5982614 A	☒	Docking station including a port replicator for sharing peripherals between a portable computer and desktop computer	361/686
31	US 5971632 A	☒	Printer with internal document data construction	400/68
32	US 5963746 A	☒	Fully distributed processing memory element	712/20
33	US 5963077 A	☒	Auto mode selector	327/408
34	US 5959869 A	☒	Vending machine controller and system	700/231
35	US 5958024 A	☒	System having a receive data register for storing at least nine data bits of frame and status bits indicating the status of asynchronous serial receiver	710/26
36	US 5949984 A	☒	Emulator system	703/23
37	US 5949780 A	☒	Integration of intelligence with communications in a switching node	370/389
38	US 5941775 A	☒	Data processing system, method thereof and memory cassette	463/44
39	US 5938736 A	☒	Search engine architecture for a high performance multi-layer switch element	709/243
40	US 5933429 A	☒	Multipoint-to-multipoint echo processing in a network switch	370/392
41	US 5923654 A	☒	Network switch that includes a plurality of shared packet buffers	370/390
42	US 5910978 A	☒	Audio/modem interface unit	379/93.01
43	US 5907304 A	☒	Lightweight antenna subpanel having RF amplifier modules embedded in honeycomb support structure between radiation and signal distribution networks	343/700 MS
44	US 5905725 A	☒	High speed switching device	370/389
45	US 5898787 A	☒	System for simultaneous game data and arena display control	700/92

	Document ID	U	Title	Current OR
46	US 5892974 A	☒	System for sub-data processor identifies the peripheral from supplied identification data and supplies data indicative of the kind of peripheral to main data processor	710/16
47	US 5892386 A	☒	Internal power control circuit for a semiconductor device	327/530
48	US 5877684 A	☒	Sensor equipped portable alarm device which can be used in conjunction with external alarm device	340/521
49	US 5872994 A	☒	Flash memory incorporating microcomputer having on-board writing function	712/43
50	US 5867690 A	☒	Apparatus for converting data between different endian formats and system and method employing same	710/65
51	US 5857011 A	☒	Multi-port caller ID-based telephone ringback test device	379/29.06
52	US 5852712 A	☒	Microprocessor having single poly-silicon EPROM memory for programmably controlling optional features	714/5
53	US 5850395 A	☒	Asynchronous transfer mode based service consolidation switch	370/398
54	US 5838897 A	☒	Debugging a processor using data output during idle bus cycles	714/30
55	US 5835418 A	☒	Input/output buffer memory circuit capable of minimizing data transfer required in input and output buffering operations	365/189.05
56	US 5835025 A	☒	Portable battery operated power managed event recorder and interrogator system	340/870.02
57	US 5834693 A	☒	Computer I/O support bracket and cable assembly	174/65R
58	US 5832291 A	☒	Data processor with dynamic and selectable interconnections between processor array, external memory and I/O ports	712/11
59	US 5826049 A	☒	Partial broadcast method in parallel computer and a parallel computer suitable therefor	710/317
60	US 5812879 A	☒	External multiple peripheral interface to computer serial port using individually configured parallel port terminals	710/62
61	US 5812550 A	☒	Asynchronous transfer mode (ATM) layer function processing apparatus with an enlarged structure	370/395.4
62	US 5805924 A	☒	Method and apparatus for configuring fabrics within a fibre channel system	710/11
63	US 5805589 A	☒	Central shared queue based time multiplexed packet switch with deadlock avoidance	370/389
64	US 5805085 A	☒	Apparatus and method for scanning a key matrix	341/26
65	US 5802052 A	☒	Scalable high performance switch element for a shared memory packet or ATM cell switch fabric	370/395.72
66	US 5799209 A	☒	Multi-port internally cached DRAM system utilizing independent serial interfaces and buffers arbitratively connected under a dynamic configuration	710/56
67	US 5799060 A	☒	Multi-port caller ID-based telephone ringback test device	379/29.05
68	US 5799014 A	☒	ATM cell switching system	370/358

	Document ID	U	Title	Current OR
69	US 5796675 A	☒	Synchronous memory device having dual input registers of pipeline structure in data path	365/230.08
70	US 5796639 A	☒	Method and apparatus for verifying the installation of strapping devices on a circuit board assembly	702/118
71	US 5793313 A	☒	Apparatus and method for scanning a key matrix	341/26
72	US 5787307 A	☒	Apparatus for draining off electric charges from a bus connector pins having a switch controller for controlling two switches where the second switch connects the pins to ground	710/16
73	US 5775939 A	☒	Interface assembly for peripheral accessories	439/502
74	US 5764080 A	☒	Input/output interface circuitry for programmable logic array integrated circuit devices	326/41
75	US 5754865 A	☒	Logical address bus architecture for multiple processor systems	710/241
76	US 5754792 A	☒	Switch circuit comprised of logically split switches for parallel transfer of messages and a parallel processor system using the same	709/243
77	US 5748835 A	☒	Audio signal decoding apparatus and method for a disc driving system	386/104
78	US 5732207 A	☒	Microprocessor having single poly-silicon EPROM memory for programmably controlling optional features	714/5
79	US 5732085 A	☒	Fixed length packet switching apparatus using multiplexers and demultiplexers	370/398
80	US 5724348 A	☒	Efficient hardware/software interface for a data switch	370/384
81	US 5710770 A	☒	ATM cell switching system	370/368
82	US 5689506 A	☒	Multicast routing in multistage networks	370/388
83	US 5689505 A	☒	Buffering of multicast cells in switching networks	370/388
84	US 5689500 A	☒	Multistage network having multicast routing congestion feedback	370/235
85	US 5688174 A	☒	Multiplayer interactive video gaming device	463/37
86	US 5670955 A	☒	Method and apparatus for generating directional and force vector in an input device	341/34
87	US 5668798 A	☒	Multiplexed TC sublayer for ATM switch	370/230
88	US 5651138 A	☒	Data processor with controlled burst memory accesses and method therefor	711/154
89	US 5630161 A	☒	Serial-parallel digital signal processor	712/36
90	US 5619659 A	☒	System for extending ISA bus without using dedicated device driver software by using E.sup.2 P.sup.2 interface which provides multiplexed bus signal through standard parallel port connector	710/303

	Document ID	U	Title	Current OR
91	US 5612954 A	☒	Time switch system	370/244
92	US 5610798 A	☒	Personal computer housing	361/683
93	US 5608686 A	☒	Synchronous semiconductor memory device with low power consumption	365/233
94	US 5606266 A	☒	Programmable logic array integrated circuits with enhanced output routing	326/41
95	US 5603048 A	☒	Microprocessor with bus sizing function	710/307
96	US 5598554 A	☒	Multiport series memory component	716/1
97	US 5590355 A	☒	Data driven processor, a data driven information processing device, and a method of verifying path connections of a plurality of data driven processors in such a data driven information processing device	712/26
98	US 5586289 A	☒	Method and apparatus for accessing local storage within a parallel processing computer	711/111
99	US 5574929 A	☒	Processor circuit comprising a first processor, a memory and a peripheral circuit, and system comprising the processor circuit and a second processor	712/30
100	US 5571998 A	☒	Function switching device for information processing apparatus	200/50.28
101	US 5565879 A	☒	High scan rate low sidelobe circular scanning antenna	343/781R
102	US 5561822 A	☒	System status maintaining and supporting apparatus sharing one console with a CPU	710/36
103	US 5561384 A	☒	Input/output driver circuit for isolating with minimal power consumption a peripheral component from a core section	327/108
104	US 5559970 A	☒	Crossbar switch for multi-processor, multi-memory system for resolving port and bank contention through the use of aligners, routers, and serializers	710/317
105	US 5555436 A	☒	Apparatus for allowing multiple parallel port devices to share a single parallel port	710/1
106	US 5546391 A	☒	Central shared queue based time multiplexed packet switch with deadlock avoidance	370/413
107	US 5539223 A	☒	Wiring structure of source line used in semicustom integrated circuit	257/207
108	US 5532938 A	☒	Numerical arithmetic processing unit	708/524
109	US 5532844 A	☒	Image data transferring system and method	358/468
110	US 5506840 A	☒	Asynchronous switching node and routing logic means for a switching element used therein	370/397
111	US 5504882 A	☒	Fault tolerant data storage subsystem employing hierarchically arranged controllers	714/5
112	US 5500611 A	☒	Integrated circuit with input/output pad having pullup or pulldown	326/87

	Document ID	U	Title	Current OR
113	US 5497471 A	☒	High performance computer system which minimizes latency between many high performance processors and a large amount of shared memory	711/100
114	US 5497292 A	☒	Configurable computer chassis port and method of manufacture therefor	361/818
115	US 5488695 A	☒	Video peripheral board in expansion slot independently exercising as bus master control over system bus in order to relief control of host computer	710/110
116	US 5455468 A	☒	Switching circuit for switching a plurality of lines	307/112
117	US 5444700 A	☒	Switching element and method for controlling the same	370/351
118	US 5442800 A	☒	Parallel input-output circuit permitting reduce number of pins in a single chip microcomputer	712/38
119	US 5436183 A	☒	Electrostatic discharge protection transistor element fabrication process	438/200
120	US 5422493 A	☒	Asynchronous bidirectional node switch	250/551
121	US 5420986 A	☒	FDDI concentrator with backplane port for dual datapath systems	370/452
122	US 5418891 A	☒	Printer sharing device	358/1.15
123	US 5417222 A	☒	Patient monitoring system	600/509
124	US 5416161 A	☒	Semiconductor integrated circuit device	361/56
125	US 5412261 A	☒	Two-stage programmable interconnect architecture	264/41
126	US 5408668 A	☒	Method and apparatus for controlling the provision of power to computer peripherals	713/324
127	US 5392329 A	☒	Automatic call distribution system with emergency recording system and method	379/49
128	US 5381553 A	☒	Signal processing apparatus for performing high speed arithmetic operations and having a power consumption reduction feature	713/320
129	US 5377357 A	☒	Connection state confirmation system and method for expansion unit	710/303
130	US 5375209 A	☒	Microprocessor for selectively configuring pinout by activating tri-state device to disable internal clock from external pin	703/25
131	US 5369643 A	☒	Method and apparatus for mapping test signals of an integrated circuit	714/724
132	US 5365519 A	☒	ATM switching system connectable to I/O links having different transmission rates	370/378
133	US 5359717 A	☒	Microprocessor arranged to access a non-multiplexed interface or a multiplexed peripheral interface	710/305
134	US 5348500 A	☒	Marine propulsion device with selectively operable secondary exhaust discharge	440/89R
135	US 5345409 A	☒	Programmable digital signal processor system for processing electrical power signals	702/60

	Document ID	U	Title	Current OR
136	US 5345228 A	☒	Very large scale modular switch	340/2.25
137	US 5329520 A	☒	High-speed facility protection in a digital telecommunications system	370/225
138	US 5317748 A	☒	Information processing apparatus for performing two-way interruption processing	710/260
139	US 5317210 A	☒	I/O cell for programmable logic device providing latched, unlatched, and fast inputs	326/40
140	US 5309430 A	☒	Telecommunication system	370/397
141	US 5309426 A	☒	High performance cascadable simplex switch	370/427
142	US 5303246 A	☒	Fault isolation diagnostics	714/727
143	US 5293489 A	☒	Circuit arrangement capable of centralizing control of a switching network	710/317
144	US 5266951 A	☒	Analog to digital converter calibration system and method of operation	341/120
145	US 5253345 A	☒	Point of sale register system	705/17
146	US 5249178 A	☒	Routing system capable of effectively processing routing information	370/392
147	US 5210742 A	☒	Communication process and switching element for carrying out this process	370/400
148	US 5189665 A	☒	Programmable configurable digital crossbar switch	370/248
149	US 5175702 A	☒	Digital signal processor architecture with plural multiply/accumulate devices	708/523
150	US 5140773 A	☒	Microprocessor controlled door holder	307/125
151	US 5138702 A	☒	External image input/output device connectable image processing system	710/37
152	US 5130975 A	☒	Dual port memory buffers and a time slot scheduler for an ATM space division switching system	370/416
153	US 5123011 A	☒	Modular multistage switch for a parallel computing system	370/380
154	US 5111508 A	☒	Audio system for vehicular application	381/100
155	US 5093878 A	☒	Asynchronous time division switch with increased traffic handling capability	370/422
156	US 5051622 A	☒	Power-on strap inputs	326/38
157	US 5034686 A	☒	Weapon interface system evaluation apparatus and method	324/537
158	US 5027346 A	☒	Node apparatus for parallel communication	370/360

	Document ID	U	Title	Current OR
159	US 5025361 A	☒	Watering control system	700/14
160	US 4991197 A	☒	Method and apparatus for controlling transmission of voice and data signals	455/557
161	US 4947357 A	☒	Scan testing a digital system using scan chains in integrated circuits	714/726
162	US 4945267 A	☒	Integrated circuit bus switching circuit	327/434
163	US 4924426 A	☒	Apparatus with selection circuitry for distributing data blocks from external memory to processing units according to attribute data contained in each data block	711/100
164	US 4924399 A	☒	Vehicle control system with HSO-triggered output	701/101
165	US 4910703 A	☒	Data processing unit having multiple-purpose port used as a resonator connection port in first mode and as a data i/o port in second mode	713/500
166	US 4910665 A	☒	Distributed processing system including reconfigurable elements	712/15
167	US 4905230 A	☒	Token ring expander and/or hub	370/222
168	US 4862452 A	☒	Digital signal processing system	370/263
169	US 4849931 A	☒	Data processing system having interfacing circuits assigned to a common I/O port address by utilizing a specific bit line of a common bus	710/3
170	US 4847751 A	☒	Multi-task execution control system	718/107
171	US 4845660 A	☒	Processor for signal processing and hierarchical multiprocessing structure including at least one such processor	712/35
172	US 4779079 A	☒	Multi-purpose computer utility arrangement	345/168
173	US 4766475 A	☒	Semiconductor integrated circuit device having an improved buffer arrangement	257/203
174	US 4761762 A	☒	Interrupt control switch interface system	710/260
175	US 4710868 A	☒	Interconnect scheme for shared memory local networks	710/316
176	US 4696059 A	☒	Reflex optoelectronic switching matrix	398/55
177	US 4672537 A	☒	Data error detection and device controller failure detection in an input/output system	714/56
178	US 4672535 A	☒	Multiprocessor system	710/38
179	US 4623996 A	☒	Packet switched multiple queue NXM switch node and processing method	370/418
180	US 4554530 A	☒	Method and apparatus for scanning a matrix of switchable elements	341/26
181	US 4539676 A	☒	Bulk/interactive data switching system	370/354

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182	US 4503497 A	☒	System for independent cache-to-cache transfer	711/124
183	US 4491838 A	☒	Starloop communication network and control system therefor	370/407
184	US 4459660 A	☒	Microcomputer with automatic refresh of on-chip dynamic RAM transparent to CPU	711/1
185	US 4458841 A	☒	Function control module for air treating systems	236/49.4
186	US 4450521 A	☒	Digital processor or microcomputer using peripheral control circuitry to provide multiple memory configurations and offset addressing capability	710/3
187	US 4435763 A	☒	Multiprogrammable input/output circuitry	703/27
188	US 4405978 A	☒	Microprocessor based computer terminal	710/67
189	US 4363108 A	☒	Low cost programmable video computer terminal	345/467
190	US 4276451 A	☒	Control system for telephone switching system	379/15.05
191	US 4177511 A	☒	Port select unit for a programmable serial-bit microprocessor	710/37
192	US 4155056 A	☒	Cascaded grating resonator filters with external input-output couplers	333/195
193	US 4145760 A	☒	Memory device having a reduced number of pins	365/226
194	US 4017840 A	☒	Method and apparatus for protecting memory storage location accesses	711/164
195	US 3922537 A	☒	Multiplex device for automatic test equipment	714/32
196	US 3916384 A	☒	Communication switching system computer memory control arrangement	711/149
197	US 3845425 A	☒	METHOD AND APPARATUS FOR PROVIDING CONDITIONAL AND UNCONDITIONAL ACCESS TO PROTECTED MEMORY STORAGE LOCATIONS	711/152
198	US 3725621 A	☐	MULTI-CONTACT DATA MODULE HAVING A CONNECTION MATRIX AND A SWITCHING BODY AND ACTUATOR PLUG TEMPLATE	200/46

	Document ID	U	Title	Current OR
1	US 20040017132 A1	☐	Multiplexer for a piezo ceramic identification device	310/317
2	US 20040008674 A1	☒	Digital cross connect switch matrix mapping method and system	370/388
3	US 20040000676 A1	☒	Semiconductor device	257/198
4	US 20030237074 A1	☒	Microprocesser with trace module	717/124
5	US 20030234661 A1	☒	Semiconductor device and test method for the same	324/765
6	US 20030210034 A1	☒	Apparatus and methods for testing circuit boards	324/158.1
7	US 20030202474 A1	☒	Frame-pull flow control in a fibre channel network	370/235
8	US 20030197808 A1	☒	Power-on detection of DVI receiver IC	348/554
9	US 20030193939 A1	☒	SYSTEM AND METHOD FOR ASYNCHRONOUS SWITCHING OF COMPOSITE CELLS, AND CORRESPONSING INPUT PORT AND OUTPUT PORT MODULES	370/389
10	US 20030193936 A1	☒	Scalable switching fabric	370/360
11	US 20030193927 A1	☒	Random access memory architecture and serial interface with continuous packet handling capability	370/351
12	US 20030185387 A1	☒	Interworking interface module for telecommunication switching systems	379/413.02
13	US 20030180973 A1	☒	Methods and systems for monitoring a parameter of a measurement device during polishing, damage to a specimen during polishing, or a characteristic of a polishing pad or tool	438/14
14	US 20030179618 A1	☒	Internal voltage generating apparatus for a semiconductor memory device	365/200
15	US 20030174935 A1	☒	Channel balancer for WDM optical units	385/24
16	US 20030153988 A1	☒	Highly versatile process control system controller	700/19
17	US 20030142668 A1	☒	Trunking in a matrix	370/389

	Document ID	U	Title	Current OR
18	US 20030138254 A1	☒	Light branching/inserting apparatus and light branching apparatus using wavelength selection filter	398/85
19	US 20030135706 A1	☒	Microcontroller having embedded non-volatile memory with read protection	711/163
20	US 20030128715 A1	☒	MULTI-SERVICE ARCHITECTURE WITH ANY PORT ANY SERVIVICE (APAS) HARDWARE PLATFORM	370/442
21	US 20030123440 A1	☒	ATM cell switching system	370/391
22	US 20030120970 A1	☒	Method and apparatus for debugging an electronic product using an internal I/O port	714/25
23	US 20030118275 A1	☒	Multi-dimensional optical cross-connect switching system	385/17
24	US 20030118013 A1	☒	Technique for computing pathways in a multi-stage switch fabric through exploitation of symmetrical links	370/388
25	US 20030117695 A1	☒	Connection discovery for optical amplifier systems	359/337
26	US 20030115520 A1	☒	Method for outputting error signals via monitor connect port and the computer system thereof	714/724
27	US 20030103511 A1	☒	Autoconfiguration of control connections in an exchange	370/396
28	US 20030091069 A1	☒	Multiple frequency receiver/player	370/487
29	US 20030086428 A1	☒	Switching unit for a packet-transmitting network, to switch the packets of a connection at one input of said connections' ports to at least one of its outputs	370/395.1
30	US 20030079040 A1	☒	Method and system for intelligently forwarding multicast packets	709/238
31	US 20030078752 A1	☒	SYSTEM AND METHOD FOR TESTING A CIRCUIT IMPLEMENTED ON A PROGRAMMABLE LOGIC DEVICE	702/120
32	US 20030074510 A1	☒	Method and apparatus for sharing signal pins on an interface between a system controller and peripheral integrated circuits	710/305
33	US 20030065858 A1	☒	Input apparatus of a hand-held information processing device	710/303
34	US 20030058835 A1	☒	Cross-connect control apparatus and method for broadband digital cross-connect system	370/351

	Document ID	U	Title	Current OR
35	US 20030038618 A1	☒	Network analyzer using time sequenced measurements	324/76.53
36	US 20030033433 A1	☒	Processing satellite web proxy cache	709/246
37	US 20030032311 A1	☒	Motherboard with multiple power supply selectivity	439/76.1
38	US 20030031171 A1	☒	Parallel and iterative algorithm for switching data packets	370/360
39	US 20030030459 A1	☒	Apparatus and methods for testing circuit boards	324/761
40	US 20030021522 A1	☒	Wavelength cross-connect	385/17
41	US 20030014572 A1	☒	Apparatus for merging a plurality of data streams into a single data stream	710/52
42	US 20020176657 A1	☒	Beam convergence system for optical switching cores	385/18
43	US 20020176414 A1	☒	Packet switching apparatus	370/389
44	US 20020174251 A1	☒	Method and system for connecting virtual cicuits across an ethernet switch	709/249
45	US 20020172451 A1	☒	Apparatus and method for fabricating scalable optical fiber cross-connect core	385/16
46	US 20020162063 A1	☒	Hierarchical access of test access ports in embedded core integrated circuits	714/724
47	US 20020154361 A1	☒	Wavelength division multiplexed (WDM) network element and a method for propagating data packets across the network element	398/101
48	US 20020147851 A1	☒	Multi-processor system apparatus	709/249
49	US 20020146022 A1	☒	Credit-based flow control technique in a modular multiprocessor system	370/412
50	US 20020145440 A1	☒	Semiconductor device	324/763
51	US 20020144159 A1	☒	HomePNA device with the function of transmitting power over a network wire	713/300

	Document ID	U	Title	Current OR
52	US 20020143910 A1	☒	Network hub	709/223
53	US 20020141412 A1	☒	Load balancing in link aggregation and trunking	370/392
54	US 20020131698 A1	☒	Reconfigurable optical add and drop modules with servo control and dynamic spectral power management capabilities	385/31
55	US 20020131691 A1	☒	Reconfigurable optical add-drop multiplexers employing polarization diversity	385/24
56	US 20020131690 A1	☒	Reconfigurable all-optical multiplexers with simultaneous add-drop capability	385/24
57	US 20020131688 A1	☒	Reconfigurable optical add-drop multiplexers with servo control and dynamic spectral power management capabilities	385/24
58	US 20020131687 A1	☒	Reconfigurable optical add-drop multiplexers with servo control and dynamic spectral power management capabilities	385/24
59	US 20020131442 A1	☒	SPACE/TIME SWITCH ARCHITECTURE	370/442
60	US 20020129188 A1	☒	Data processing device with memory coupling unit	710/316
61	US 20020124149 A1	☒	Efficient optimization algorithm in memory utilization for network applications	711/170
62	US 20020122387 A1	☒	Algorithm for time based queuing in network traffic engineering	370/231
63	US 20020122225 A1	☒	Multiport wavelength division multiplex network element	398/34
64	US 20020120836 A1	☒	Method for switching between boot devices in information processing unit	713/2
65	US 20020114336 A1	☒	Gateway apparatus for performing communication between WAN and LAN	370/401
66	US 20020099925 A1	☒	Apparatus and method for supporting multi-processors and motherboard of the same	712/203
67	US 20020095534 A1	☒	Method of matching cables and monitor for performing the method	710/16
68	US 20020091891 A1	☒	Passive release avoidance technique	710/311

	Document ID	U	Title	Current OR
69	US 20020071533 A1	☒	User programmable telephone wiring access terminal	379/93.05
70	US 20020064266 A1	☒	Multi-line arrangement	379/156
71	US 20020048280 A1	☒	Method and apparatus for load balancing in network processing device	370/468
72	US 20020029358 A1	☒	Method and apparatus for delivering error interrupts to a processor of a modular, multiprocessor system	714/39
73	US 20020011823 A1	☒	Smart battery, secondary smart battery connection apparatus of portable computer system, AC adapter implementing same, and connection method thereof	320/137
74	US 20020010872 A1	☒	Multi-agent synchronized initialization of a clock forwarded interconnect based computer system	713/400
75	US 20020009095 A1	☒	Multicast decomposition mechanism in a hierarchically order distributed shared memory multiprocessor computer system	370/432
76	US 20020001305 A1	☒	Flexible, self-aligning time and space switch fabrics	370/369
77	US 20010055277 A1	☒	Initiate flow control mechanism of a modular multiprocessor system	370/236
78	US 20010050916 A1	☒	METHOD AND APPARATUS FOR PROVIDING WORK-CONSERVING PROPERTIES IN A NON-BLOCKING SWITCH WITH LIMITED SPEEDUP INDEPENDENT OF SWITCH SIZE	370/419
79	US 20010049801 A1	☒	Dual-ported operator control panel with automatic failover	714/10
80	US 20010043597 A1	☒	ATM CELL SWITCHING SYSTEM	370/368
81	US 20010040485 A1	☒	Switch assembly with a multi-pole switch for combining amplified RF signals to a single RF signal	333/101
82	US 20010038759 A1	☒	Method and system for information control capable of effectively performing an automatic payment for maintenance expenses	399/79
83	US 20010034142 A1	☒	Signal transmission connector and cable employing same	439/55
84	US 20010028652 A1	☒	ATM cell switching system	370/395.1
85	US 20010021659 A1	☒	Method and system for connecting a mobile communication unit to a personal computer	455/557

	Document ID	U	Title	Current OR
86	US 20010 00569 1 A1	☒	Multiplayer interactive video gaming device	463/42
87	US 20010 00538 6 A1	☒	ATM cell switching system	370/538
88	US 66874 31 B2	☒	Reconfigurable optical add-drop multiplexers with servo control and dynamic spectral power management capabilities	385/24
89	US 66872 46 B1	☒	Scalable switching fabric	370/388
90	US 66870 44 B2	☒	Connection discovery for optical amplifier systems	359/337
91	US 66842 35 B1	☒	One-dimensional wavelet system and method	708/400
92	US 66782 87 B1	☒	Method for multiplexing signals through I/O pins	370/546
93	US 66691 00 B1	☒	Serviceable tamper resistant PIN entry apparatus	235/492
94	US 66619 48 B2	☒	Reconfigurable optical add and drop modules with servo control and dynamic spectral power management capabilities	385/24
95	US 66612 73 B1	☒	Substrate pump circuit and method for I/O ESD protection	327/310
96	US 66549 13 B1	☒	Alternate port apparatus for manufacturing test of integrated serial bus and method therefor	714/43
97	US 66508 03 B1	☒	Method and apparatus for optical to electrical to optical conversion in an optical cross-connect switch	385/17
98	US 66486 52 B2	☒	Signal transmission connector and cable employing same	439/55
99	US 66469 83 B1	☒	Network switch which supports TDM, ATM, and variable length packet traffic and includes automatic fault/congestion correction	370/218
100	US 66393 93 B2	☒	Methods and apparatus for time-domain measurement with a high frequency circuit analyzer	324/76.19
101	US 66365 15 B1	☒	Method for switching ATM, TDM, and packet data through a single communications switch	370/395.1
102	US 66365 11 B1	☒	Method of multicasting data through a communications switch	370/390
103	US 66311 30 B1	☒	Method and apparatus for switching ATM, TDM, and packet data through a single communications switch while maintaining TDM timing	370/352
104	US 66253 46 B2	☒	Reconfigurable optical add-drop multiplexers with servo control and dynamic spectral power management capabilities	385/24
105	US 66186 86 B2	☒	System and method for testing a circuit implemented on a programmable logic device	702/120
106	US 66183 72 B1	☒	Packet switching system having-having self-routing switches	370/389
107	US 66147 58 B2	☒	Load balancing in link aggregation and trunking	370/232

	Document ID	U	Title	Current OR
108	US 6611518 B1	☒	Methods and apparatus for flexible device interface port assignment in a data communications switching system	370/386
109	US 6608475 B2	☒	Network analyzer using time sequenced measurements	324/76.53
110	US 6606326 B1	☒	Packet switch employing dynamic transfer of data packet from central shared queue path to cross-point switching matrix path	370/412
111	US 6597826 B1	☒	Optical cross-connect switching system with bridging, test access and redundancy	385/17
112	US 6597656 B1	☒	Switch system comprising two switch fabrics	370/219
113	US 6590225 B2	☒	Die testing using top surface test pads	257/48
114	US 6587014 B2	☒	Switch assembly with a multi-pole switch for combining amplified RF signals to a single RF signal	333/101
115	US 6584121 B1	☒	Switch architecture for digital multiplexed signals	370/474
116	US 6581841 B1	☒	Apparatus and method for secure information processing	235/492
117	US 6578185 B1	☒	Power-supply-configurable outputs	716/16
118	US 6571030 B1	☒	Optical cross-connect switching system	385/17
119	US 6570845 B1	☒	Switching system including a mask mechanism for altering the internal routing process	370/218
120	US 6564331 B1	☒	Low power register file	713/324
121	US 6563837 B2	☒	Method and apparatus for providing work-conserving properties in a non-blocking switch with limited speedup independent of switch size	370/413
122	US 6560227 B1	☒	LAN frame copy decision for LAN switches	370/390
123	US 6560205 B1	☒	Method and apparatus for control of soft handoff usage in radiocommunication	370/258
124	US 6549699 B2	☒	Reconfigurable all-optical multiplexers with simultaneous add-drop capability	385/24
125	US 6549543 B1	☒	Data communication system and data communication operating method	370/474
126	US 6546011 B1	☒	ATM cell switching system	370/391
127	US 6538782 B1	☒	Light branching/inserting apparatus and light branching apparatus using wavelength selection filter	398/82
128	US 6529478 B1	☒	Pass/drop apparatus and method for network switching node	370/236
129	US 6522669 B1	☒	Devices and methods relating to telecommunications equipment	370/498
130	US 6507117 B1	☒	Semiconductor chip and multichip-type semiconductor device	257/778

	Document ID	U	Title	Current OR
131	US 6501757 B1	☒	ATM switch	370/395.41
132	US 6496880 B1	☒	Shared I/O ports for multi-core designs	710/38
133	US 6484209 B1	☒	Efficient path based forwarding and multicast forwarding	709/238
134	US 6480924 B1	☒	Application specific integrated circuit and transceiver with multi-mode connection	710/306
135	US 6480921 B1	☒	Reducing internal bus speed in a bus system without reducing readout rate	710/305
136	US 6469651 B1	☒	Multi-function type absolute converter	341/160
137	US 6463057 B1	☒	ATM cell switching system	370/358
138	US 6459863 B2	☒	Method and system for information control capable of effectively performing an automatic payment for maintenance expenses	399/79
139	US 6449740 B1	☒	Conductive paths controllably coupling pad groups arranged along one edge to CPU and to EEPROM in test mode	714/718
140	US 6449576 B1	☒	Network processor probing and port mirroring	702/117
141	US 6445703 B2	☒	ATM cell switching system	370/391
142	US 6434115 B1	☒	System and method for switching packets in a network	370/235
143	US 6430630 B1	☒	Direct data access between input and output ports	710/22
144	US 6427914 B1	☒	Apparatus and method for operating a checkout system having a number of port expander devices associated therewith	235/383
145	US 6424226 B1	☒	Two-port with a frequency-dependent network	330/302
146	US 6417944 B1	☒	Asynchronous transfer mode switch utilizing optical wave division multiplexing	398/79
147	US 6415022 B1	☒	User programmable telephone wiring access terminal	379/93.05
148	US 6408413 B1	☒	Hierarchical access of test access ports in embedded core integrated circuits	714/727
149	US 6405273 B1	☒	Data processing device with memory coupling unit	710/305
150	US 6404225 B1	☒	Integrated circuit incorporating a programmable cross-bar switch	326/39
151	US 6396844 B1	☒	Backplane architecture for providing both loop repeater and multiplexed mode connectivity in the same equipment shelf	370/420
152	US 6396831 B1	☒	ATM cell switching system	370/358
153	US 6378065 B1	☒	Apparatus with context switching capability	712/228

	Document ID	U	Title	Current OR
154	US 6369427 B1	☒	Integrated circuitry, interface circuit of an integrated circuit device, and cascode circuitry	257/355
155	US 6363077 B1	☒	Load balancing in link aggregation and trunking	370/422
156	US 6356958 B1	☒	Integrated circuit module has common function known good integrated circuit die with multiple selectable functions	710/1
157	US 6345310 B1	☒	Architecture for a multiple port adapter having a single media access control (MAC) with a single I/O port	709/250
158	US 6339596 B1	☒	ATM cell switching system	370/395.7
159	US 6337906 B1	☒	Apparatus and method for coupling an automated attendant to a telecommunications system	379/308
160	US 6330240 B1	☒	ATM cell switching system	370/395.7
161	US 6314096 B1	☒	Packet switching system having self-routing switches	370/389
162	US 6311303 B1	☒	Monitor port with selectable trace support	714/734
163	US 6305766 B1	☒	Workstation with opening and support for personal computer	312/223.3
164	US 6304554 B1	☒	ATM system for conducting rate control of ATM traffic	370/236
165	US 6301620 B1	☒	Method of sending data from server computer, storage medium, and server computer	709/235
166	US 6285675 B1	☒	ATM cell switching system	370/391
167	US 6278254 B1	☒	Programmable and interactive motor starter	318/778
168	US 6272567 B1	☒	System for interposing a multi-port internally cached DRAM in a control path for temporarily storing multicast start of packet data until such can be passed	710/56
169	US 6263460 B1	☒	Microcontroller architecture and associated method providing for testing of an on-chip memory device	714/718
170	US 6263033 B1	☒	Baud rate granularity in single clock microcontrollers for serial port transmissions	375/370
171	US 6259694 B1	☒	Apparatus and method for configurable use of groups of pads of a system on chip	326/38
172	US 6246692 B1	☒	Packet switching fabric using the segmented ring with resource reservation control	370/438
173	US 6243382 B1	☒	Interfacing to SAR devices in ATM switching apparatus	370/395.52
174	US 6243020 B1	☒	Method and apparatus for programmably driving an LED display	340/815.4
175	US 6240075 B1	☒	Satellite communication routing arbitration techniques	370/325
176	US 6236839 B1	☒	Method and apparatus for calibrating a smart antenna array	455/67.14

	Document ID	U	Title	Current OR
177	US 6230109 B1	☒	Multiconductor continuity and intermittent fault analyzer with distributed processing and dynamic stimulation	702/109
178	US 6216167 B1	☒	Efficient path based forwarding and multicast forwarding	709/238
179	US 6215788 B1	☒	ATM cell switching system	370/391
180	US 6212597 B1	☒	Apparatus for and method of architecturally enhancing the performance of a multi-port internally cached (AMPIC) DRAM array and like	711/105
181	US 6211695 B1	☒	FPGA integrated circuit having embedded SRAM memory blocks with registered address and data input sections	326/40
182	US 6189052 B1	☒	On-chip i/o processor supporting different protocols having on-chip controller for reading and setting pins, starting timers, and generating interrupts at well defined points of time	710/48
183	US 6188686 B1	☒	Switching apparatus	370/388
184	US 6181163 B1	☒	FPGA integrated circuit having embedded SRAM memory blocks and interconnect channel for broadcasting address and control signals	326/41
185	US 6181159 B1	☒	Integrated circuit incorporating a programmable cross-bar switch	326/39
186	US 6175230 B1	☒	Circuit-board tester with backdrive-based burst timing	324/158.1
187	US 6172963 B1	☒	Flow control for switching	370/229
188	US 6172861 B1	☒	Protection circuit for semiconductor device	361/56
189	US 6167026 A	☒	Programmable error control circuit	370/222
190	US 6163867 A	☒	Input-output pad testing using bi-directional pads	714/736
191	US 6160811 A	☒	Data packet router	370/401
192	US 6157652 A	☒	Hub port with constant phase	370/407
193	US 6157643 A	☒	Switching fabric	370/389
194	US 6145024 A	☒	Input/output optical fiber serial interface link that selectively transfers data in multiplex channel path mode or high speed single channel path mode	710/14
195	US 6138219 A	☒	Method of and operating architectural enhancement for multi-port internally cached dynamic random access memory (AMPIC DRAM) systems, eliminating external control paths and random memory addressing, while providing zero bus contention for DRAM access	711/149
196	US 6131169 A	☒	Reliability of crossbar switches in an information processing system	714/7
197	US 6128666 A	☒	Distributed VLAN mechanism for packet field replacement in a multi-layered switched network element using a control field/signal for indicating modification of a packet with a database search engine	709/238

	Document ID	U	Title	Current OR
198	US 6128292 A	☒	Packet switching apparatus with multi-channel and multi-cast switching functions and packet switching system using the same	370/356
199	US 6118350 A	☒	Bus through termination circuit	333/22R
200	US 6114848 A	☐	Direct-measurement provision of safe backdrive levels	324/158.1